Google Developer Experts

UNIVERSITY OF AMSTERDAM

Training LLMs at Scale

On Parallelization Strategies and Efficiency

ESSIR Summer School

Phillip Lippe
PhD student, GDE JAX/Flax

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About me

- 4th year PhD student
  - Generative modeling, causality, reasoning
- Intern at Google DeepMind (Gemini) and Microsoft Research (AI4Science)
- Google Developer Expert for JAX/Flax
  - Practical implementation tutorials

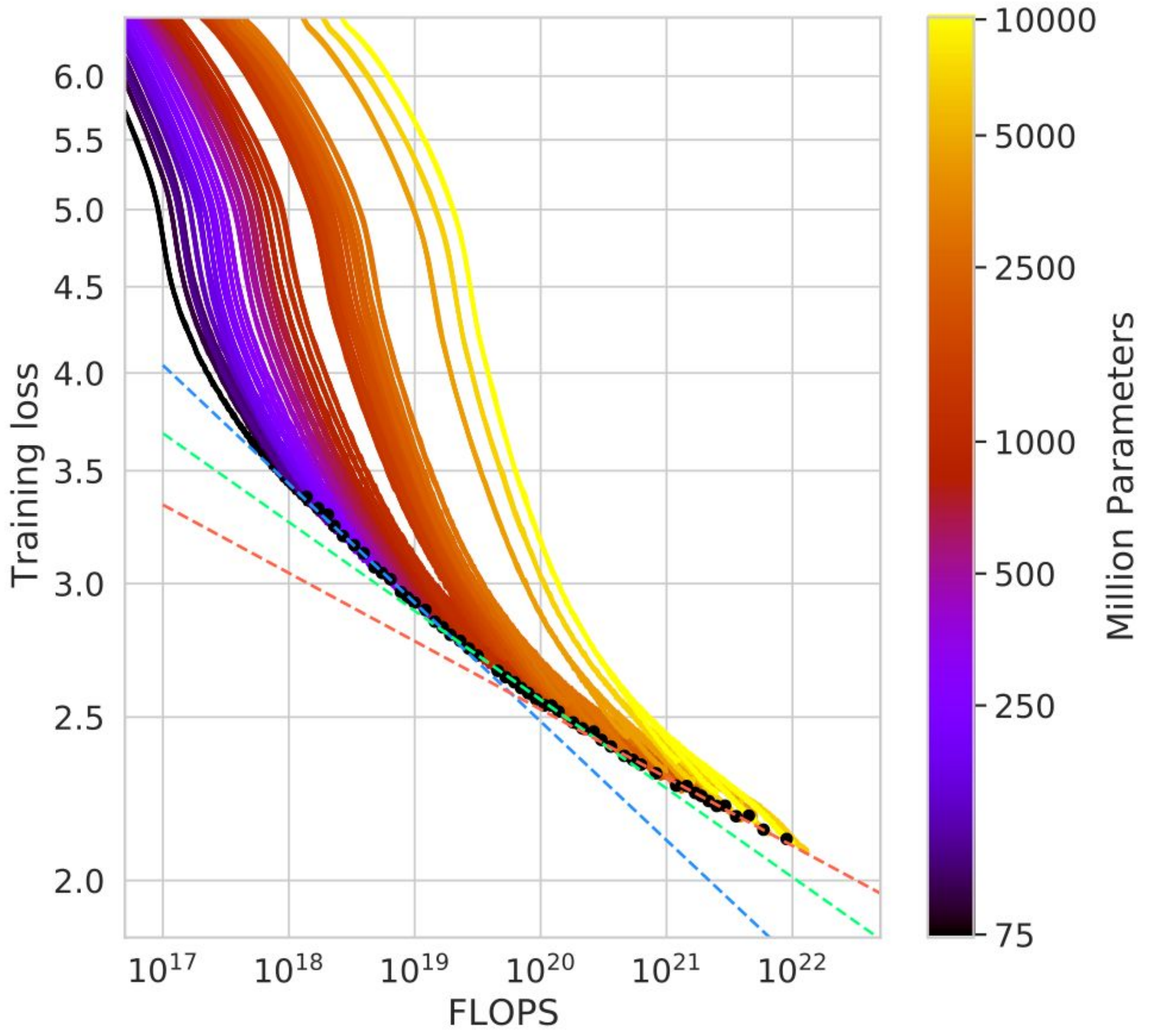
Scaling

- More FLOPs = better performance
- LLM training requires thousands of accelerators
- How do you train massive models efficiently?

Today's focus:
- Concepts and scaling strategies
- Framework agnostic

Implementation Tutorials:
[UvA-DL Notebooks]

Hoffman et al., 2022 - Chinchilla scaling laws



Scaling Challenges

- Limited resources: compute and memory
- Naive training does not fit in memory
  - How do we reduce memory usage?
- Single GPU/TPU would take years to train an LLM
  - How do we utilize maximum FLOPs of all devices?
  - Metric: MFU - Model FLOP/s utilization

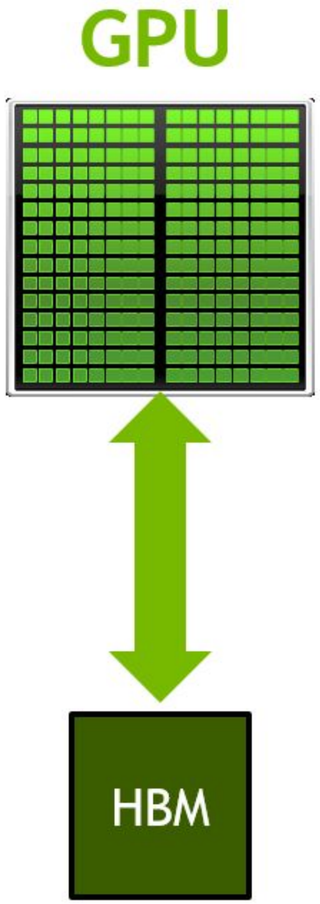
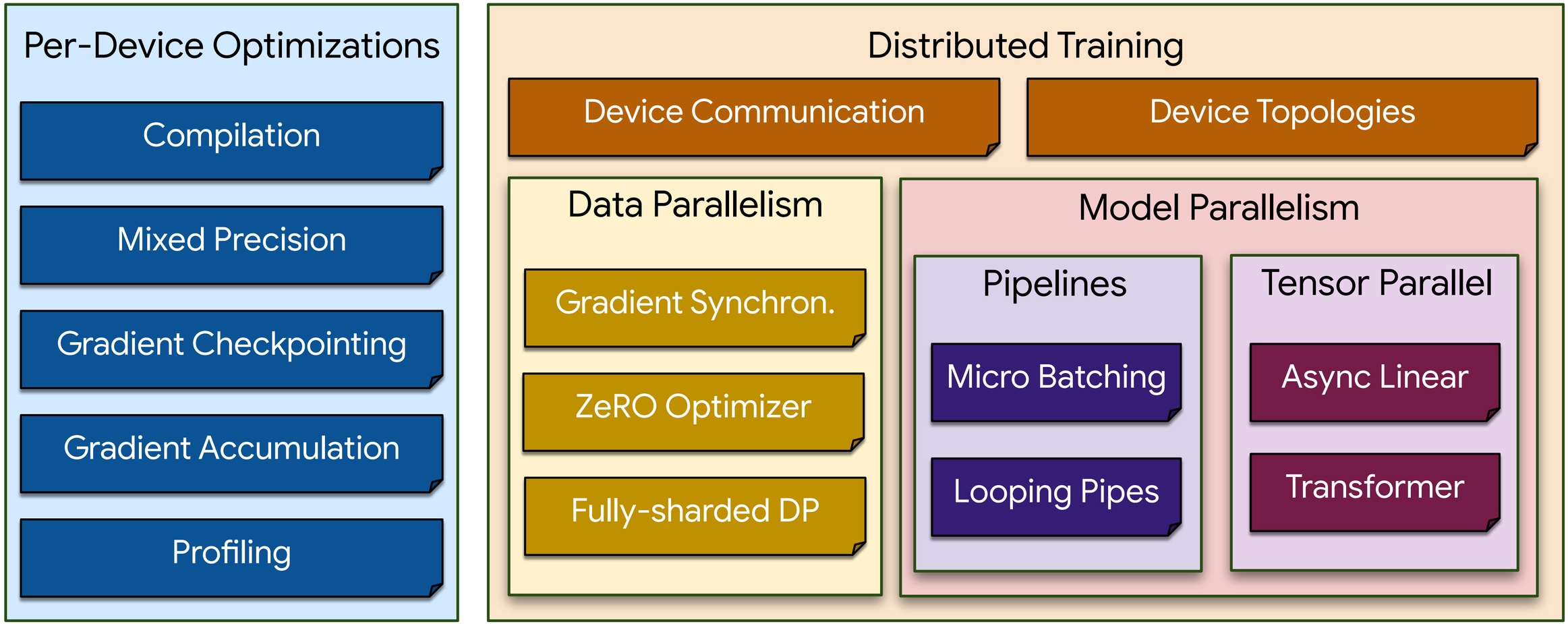


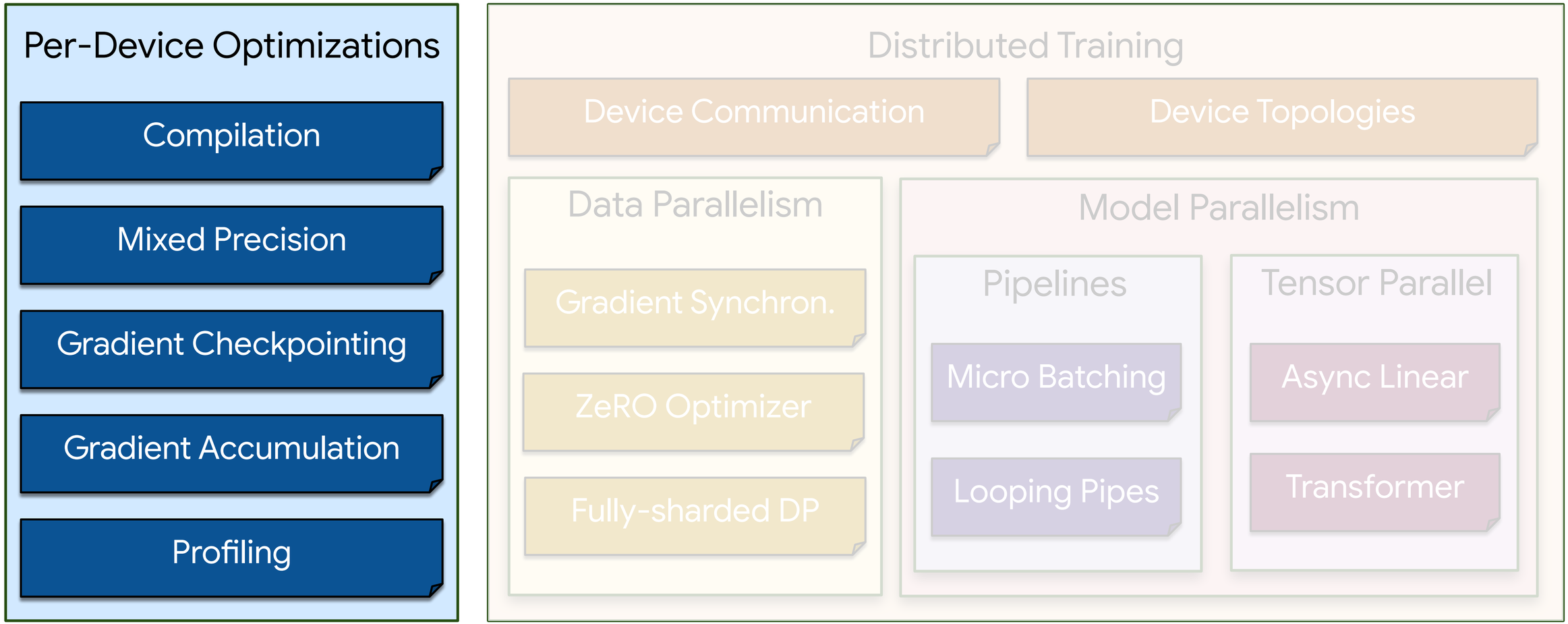
Figure credit: NVIDIA

Overview



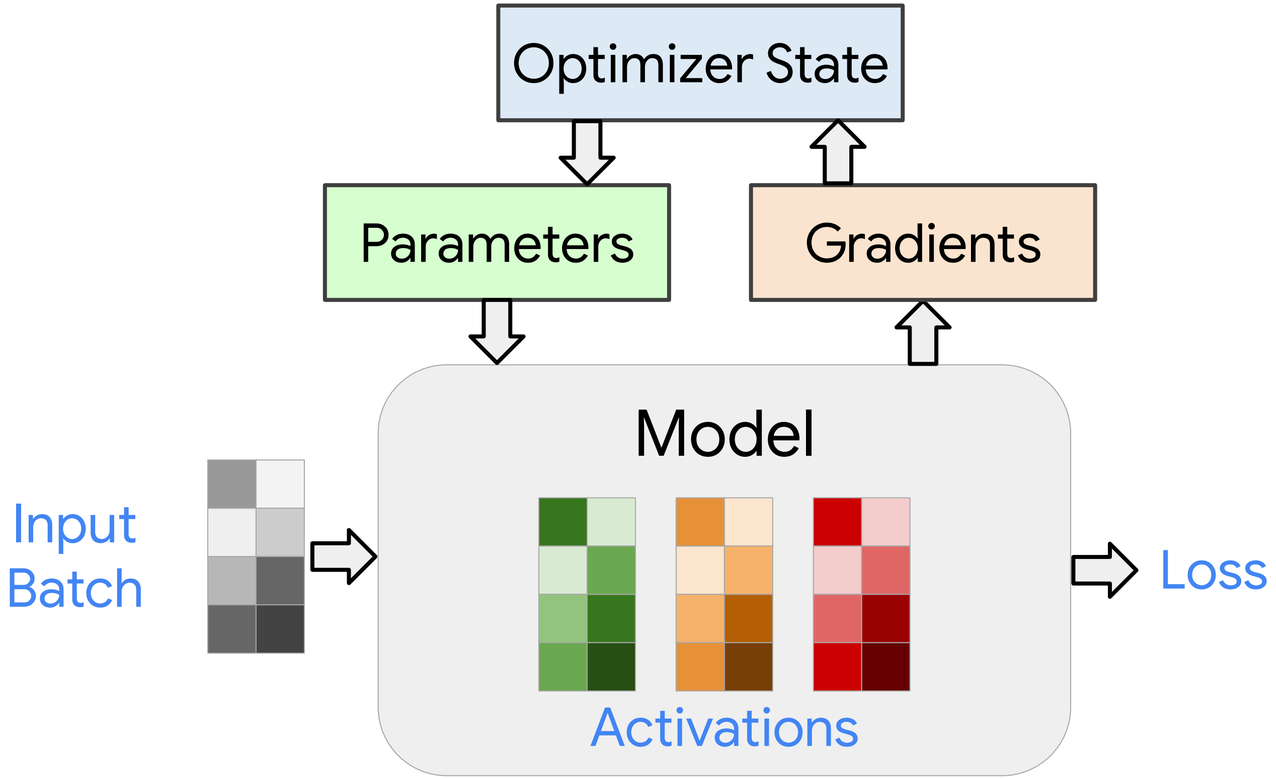
And a lot more out there...

Overview



And a lot more out there...

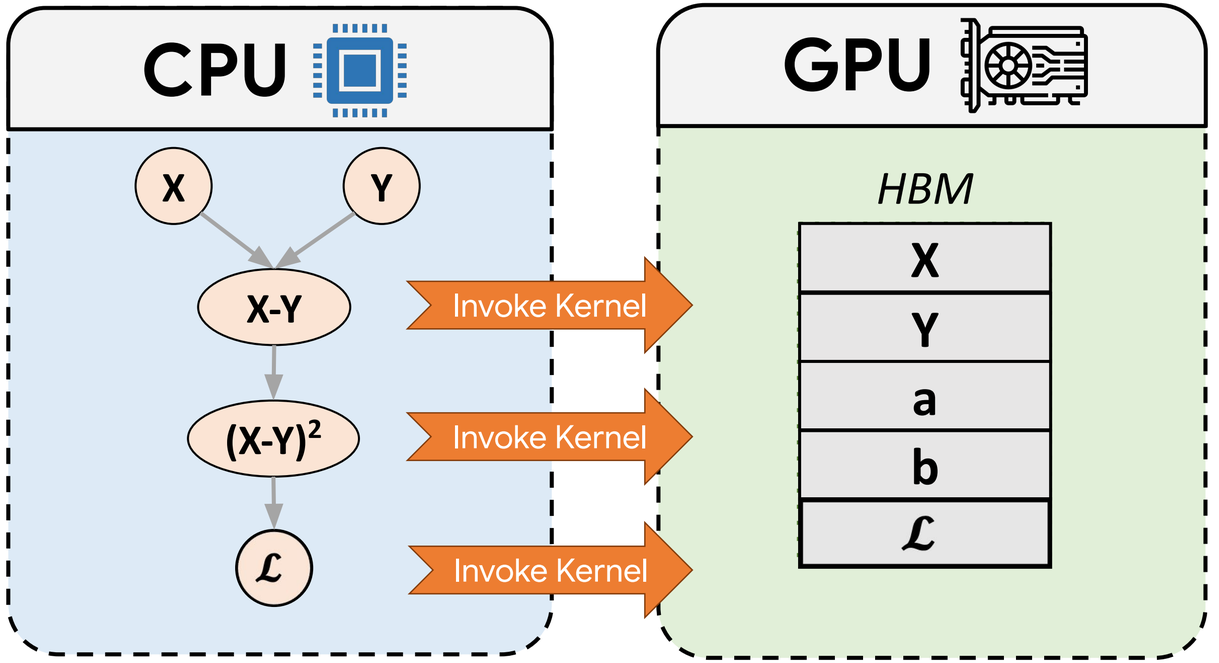
Model Training - As usual



Just-In-Time Compilation

- Execution of operations on accelerator happen asynchronously
- Eager execution requires considerable overhead in CPU ↔ GPU communication

```
def mse_loss(x, y):
    return ((x - y) ** 2).mean()
```



Just-In-Time Compilation

- Compilation fuses operations and creates fewer kernel calls
- Compiler performs accelerator-based optimizations for maximum efficiency

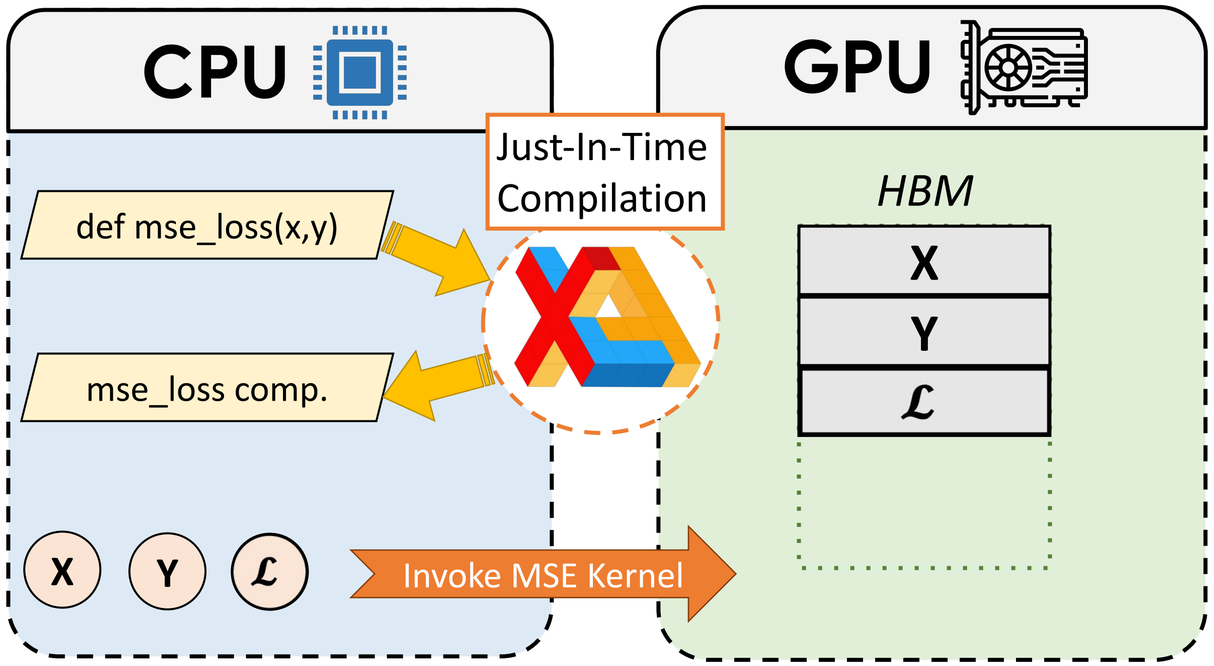
PyTorch:

- torch.compile (link)
- torch.cuda.graph (link)

JAX:

- jax.jit (link)

```
@jax.jit
def mse_loss(x, y):
    return ((x - y) ** 2).mean()
```



Low-Level Kernels

- Compilation finds general optimizations, but may not be optimal across multiple complex operations
- Most GPUs are memory-bandwidth bound (compute outspeeds memory)
- Significant gains can be achieved by minimizing memory bottleneck

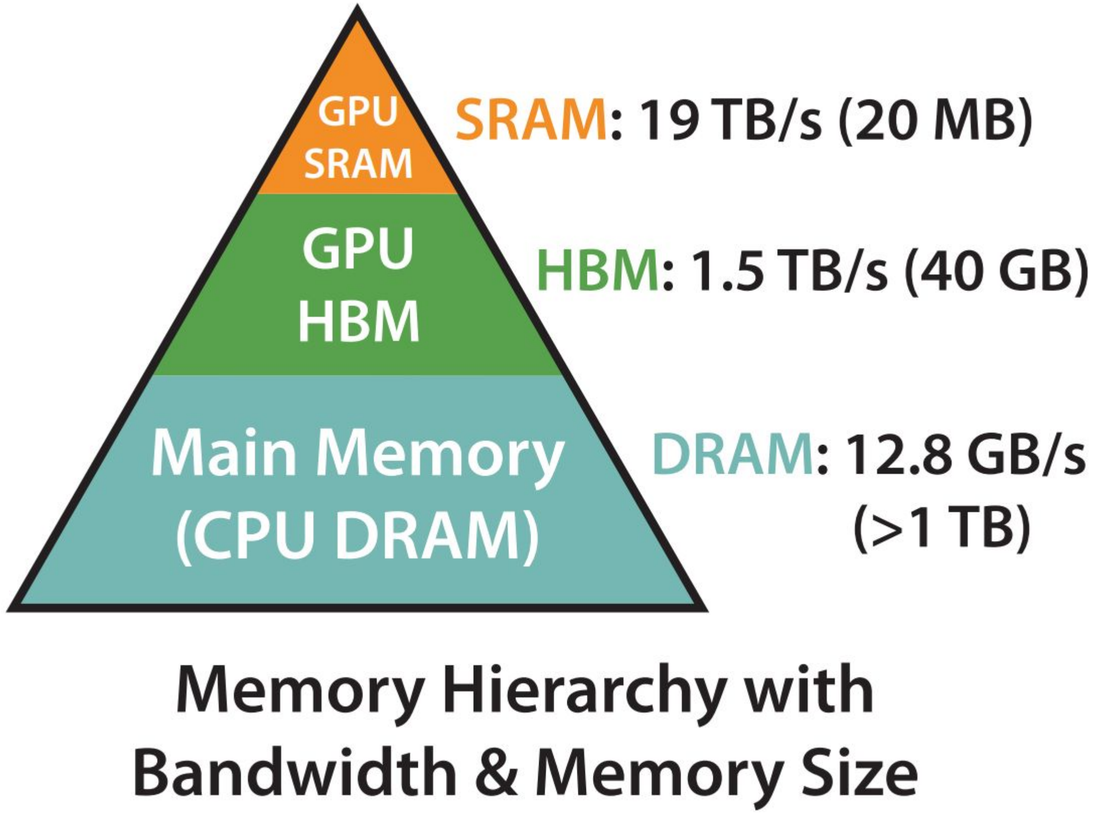
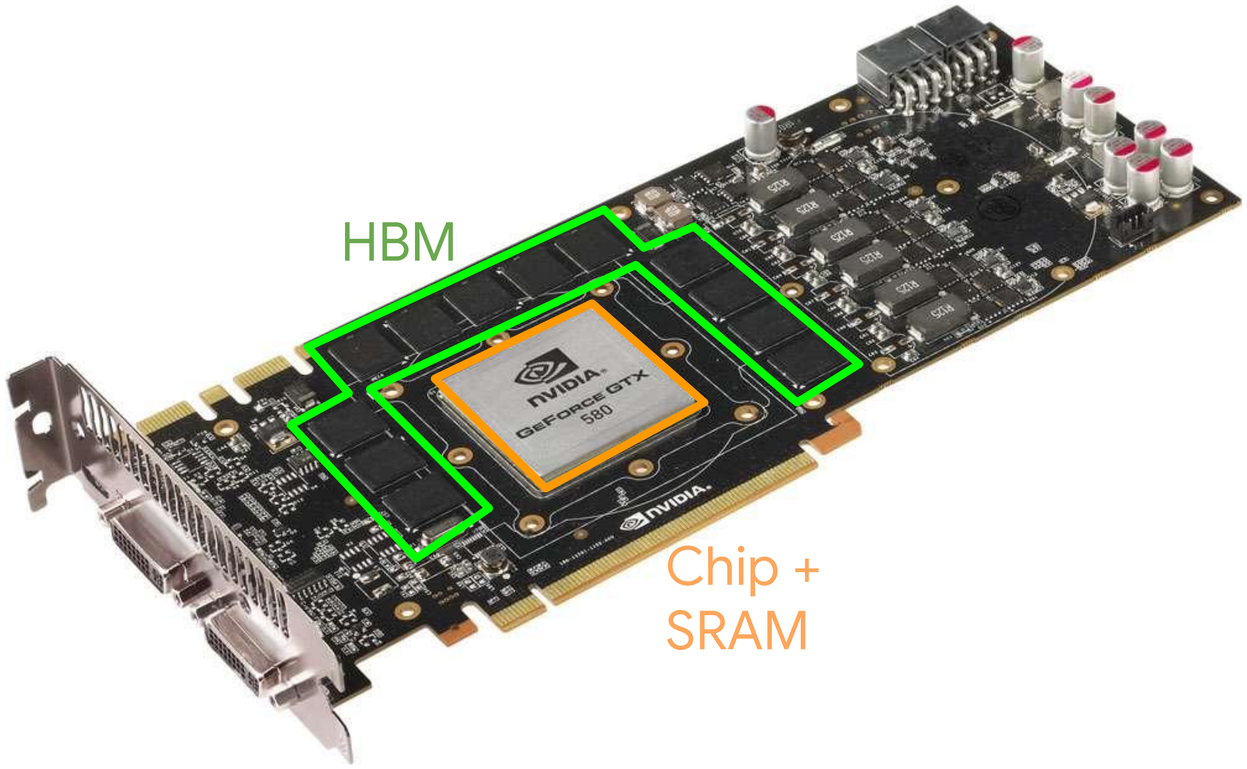
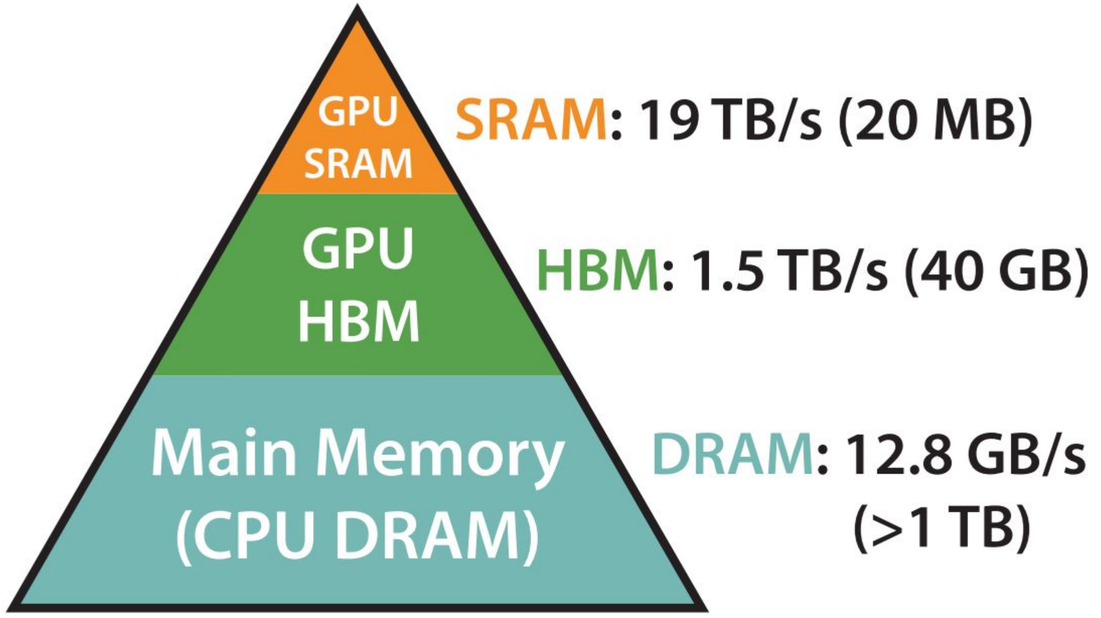


Figure credit: Dao et al., 2022

Low-Level Kernels





Memory Hierarchy with Bandwidth & Memory Size

Figure credit: Dao et al., 2022

Low-Level Kernels

- Example: Attention
- Default eager implementation:

Algorithm 0 Standard Attention Implementation

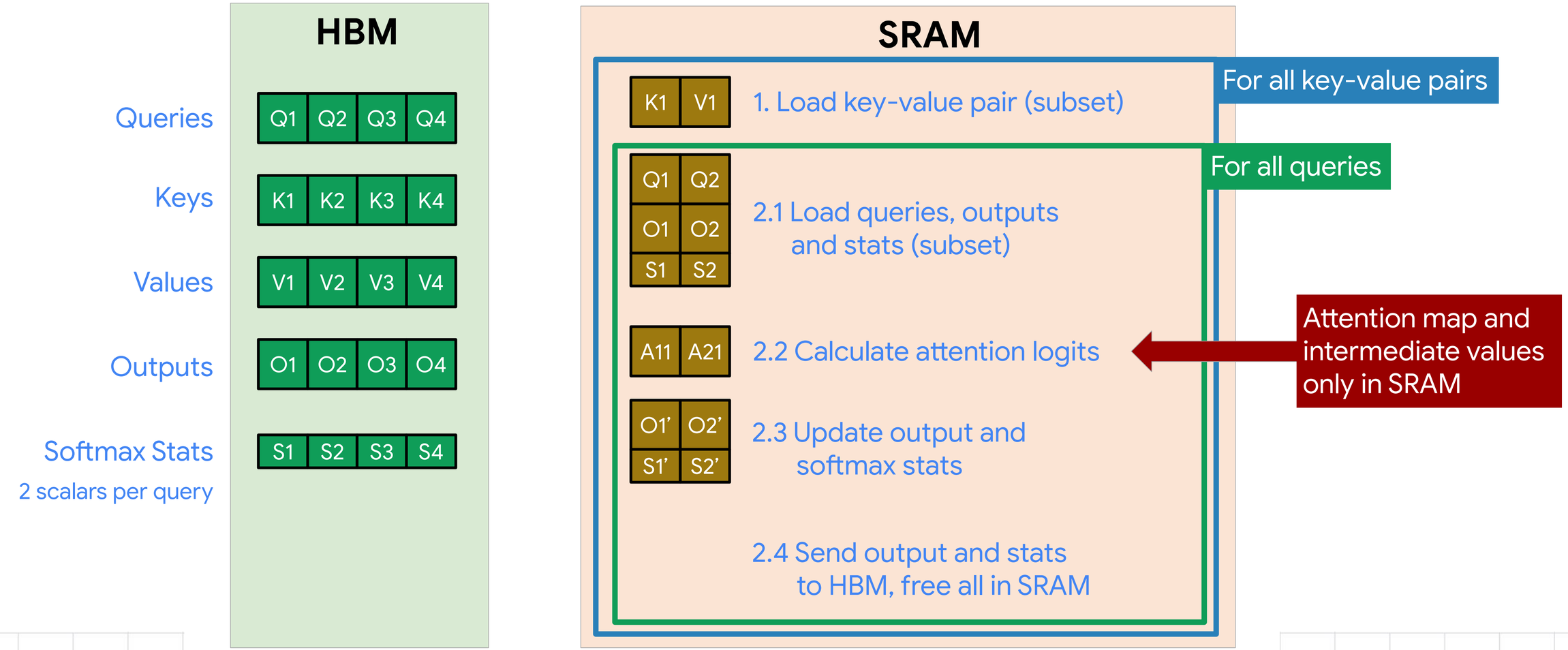
Require: Matrices $\mathbf{Q}, \mathbf{K}, \mathbf{V} \in \mathbb{R}^{N \times d}$ in HBM.

1: Load $\mathbf{Q}, \mathbf{K}$ by blocks from HBM, compute $\mathbf{S} = \mathbf{Q}\mathbf{K}^\top$, write $\mathbf{S}$ to HBM.
2: Read $\mathbf{S}$ from HBM, compute $\mathbf{P} = \mathrm{softmax}(\mathbf{S})$, write $\mathbf{P}$ to HBM.
3: Load $\mathbf{P}$ and $\mathbf{V}$ by blocks from HBM, compute $\mathbf{O} = \mathbf{P}\mathbf{V}$, write $\mathbf{O}$ to HBM.
4: Return $\mathbf{O}$.

Figure credit: Dao et al., 2022

- Several slow HBM calls - can we do better?

Flash Attention



Flash Attention

- Example: Flash Attention
- Do not materialize QK^T in HBM, but only communicate final output to HBM
- Calculate one key-value pair at a time for several queries with decomposed softmax
- Recompute attention matrix in backward
- Speedup of 3x over eager implementation
  - Compiling (esp JAX) can be similarly fast
  - Default kernel in PyTorch

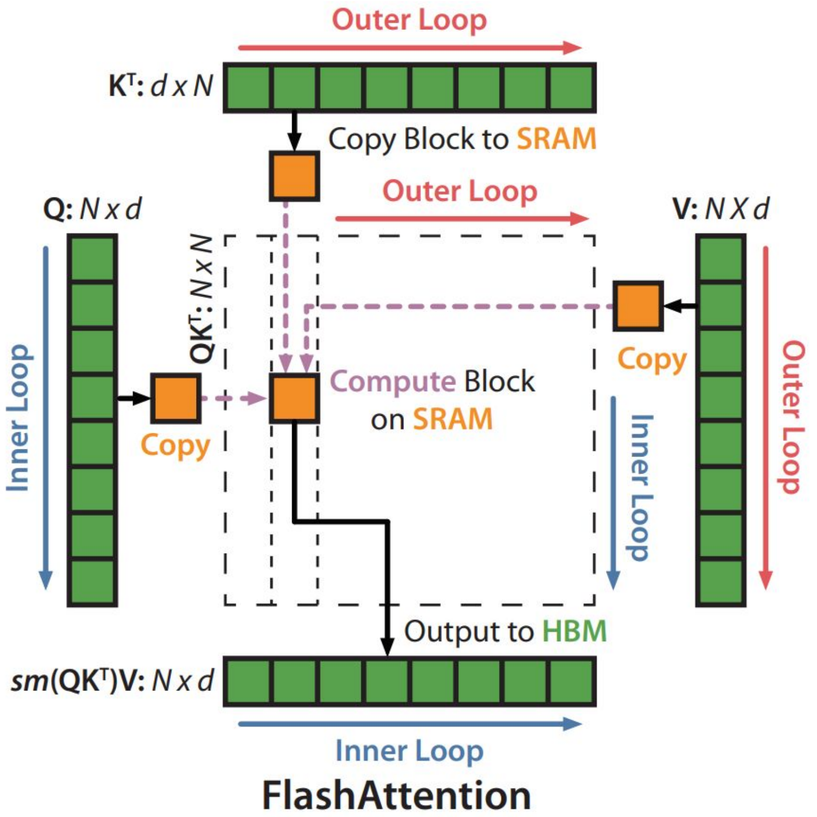


Figure credit: Dao et al., 2022

Low-Level Kernels

- Implementing low-level kernels makes new architectures viable again
- Opens up the “hardware lottery”

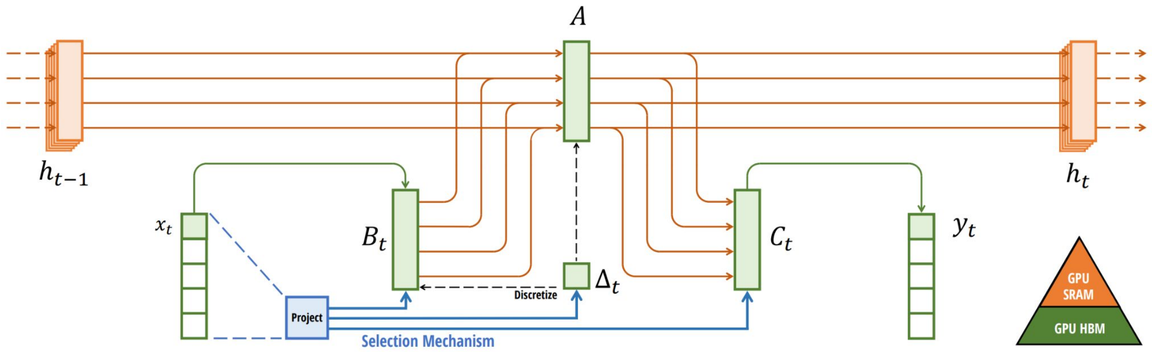


Figure credit: Gu et al., 2023

Mixed Precision

- By default, models train in float32 precision
- Modern accelerators support lower precision with significantly higher throughput

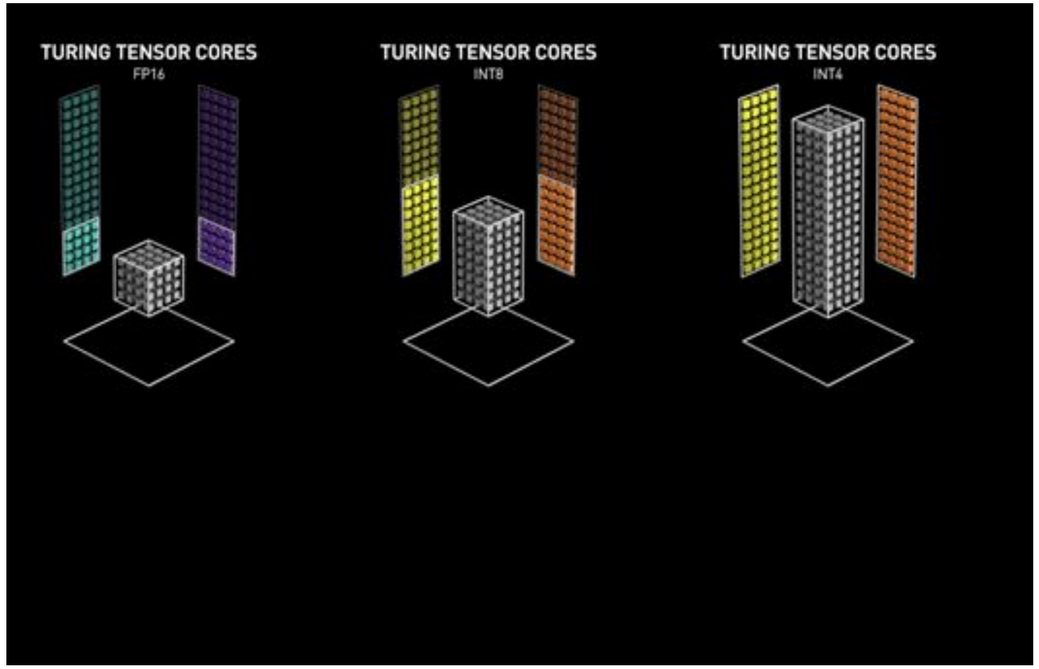


Figure credit: NVIDIA, Tensor Cores

Mixed Precision

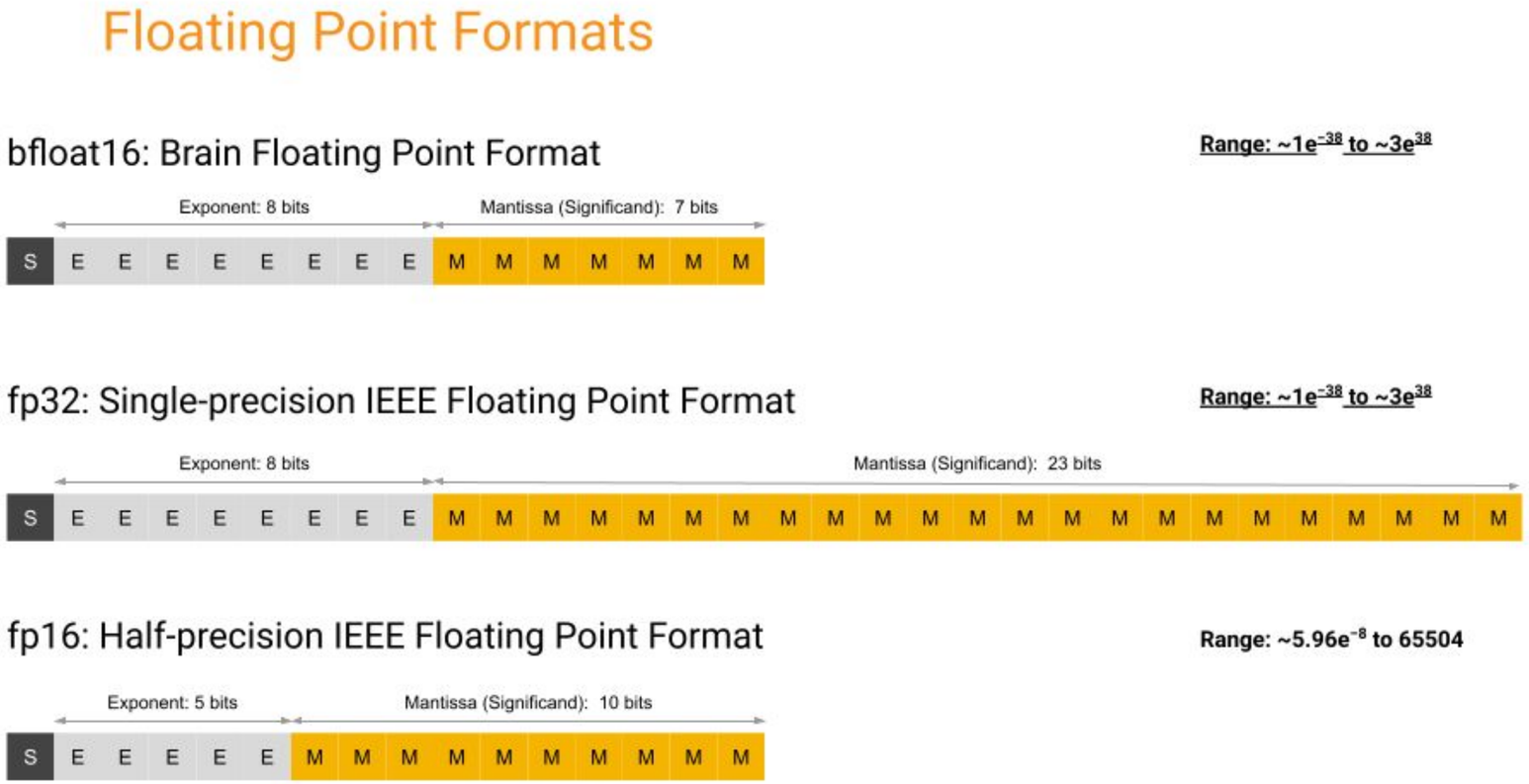
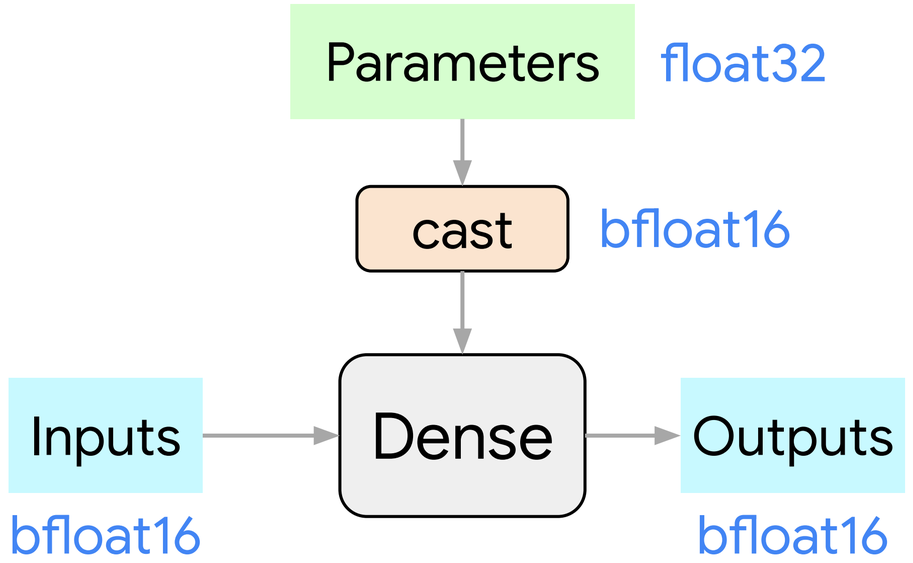


Figure credit: Google Cloud Doc

Mixed Precision

- Key idea: lower the precision of network **activations**
- Keep original parameters etc. in high precision for accurate updates
- Different precision types:
  - float16 (small range, higher precision)
  - bfloat16 (float32 range, low precision)



PyTorch:

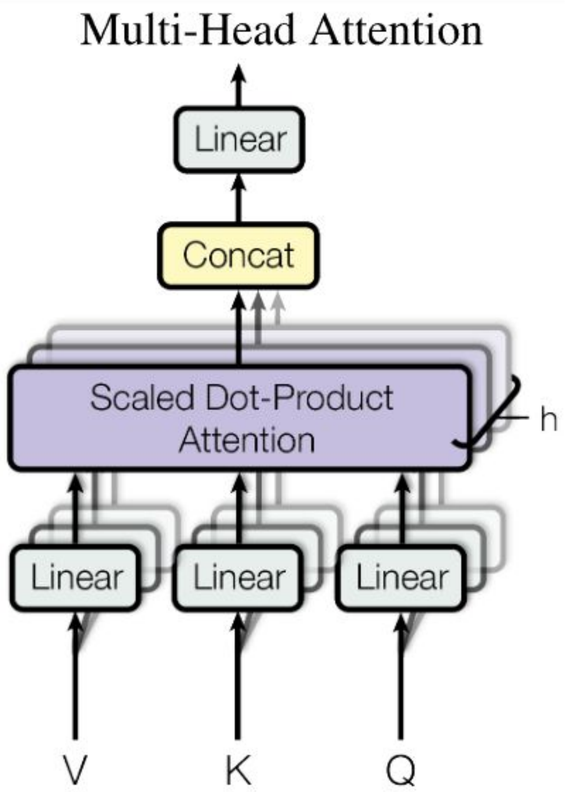
torch.autocast (link)

JAX/Flax:

Module dtype (link)

Mixed Precision

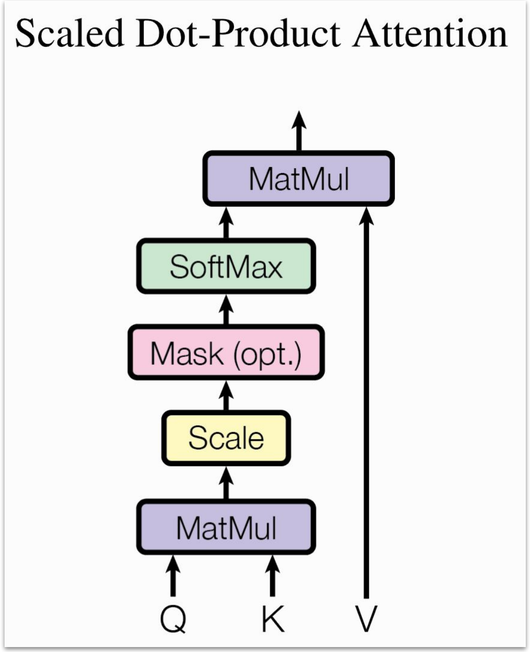
- Case study: LLM Transformer (12 layers, 155M)
- Float32: 20.6GB memory, 2.1 seconds per step
- Bfloat16: 14.6GB memory, 1.1 seconds per step
  - **30% memory reduction**, **2x speed-up**
  - Activations are 50% smaller and accelerator operates faster
  - Equivalent performance



Mixed Precision

Caveats

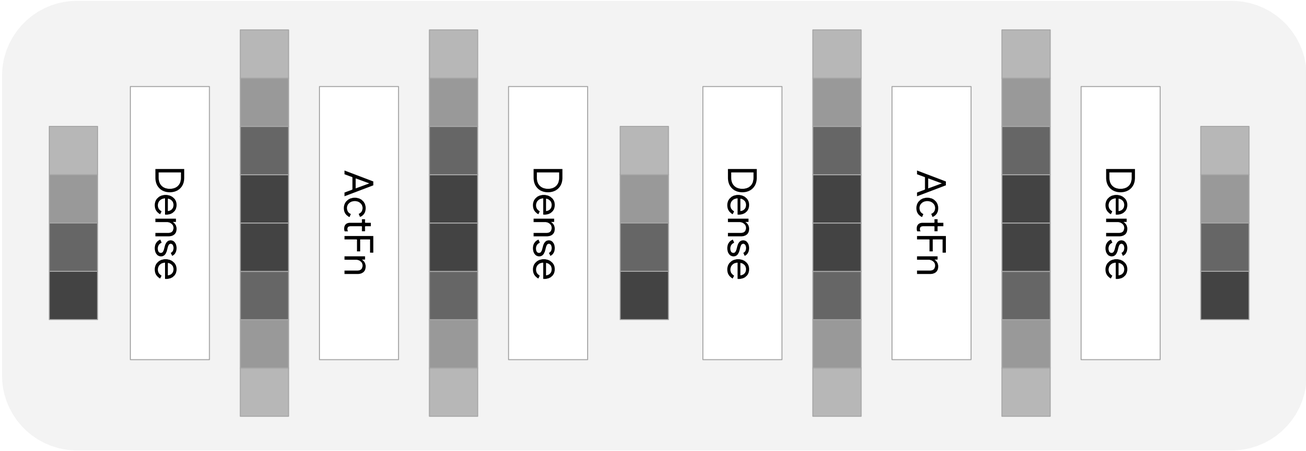
- Large reductions should be kept in high precision for numerical stability
  - Output softmax
  - Attention softmax
    - Possible with bfloat16 in smaller seq lengths
- Lower precision parameters and optimizer possible
  - More tricky, performance might suffer



Gradient Checkpointing

- Storing all activations in memory is very expensive
- Alternative: recompute activations on demand

Forward pass



Memory: O(40)

Gradient Checkpointing

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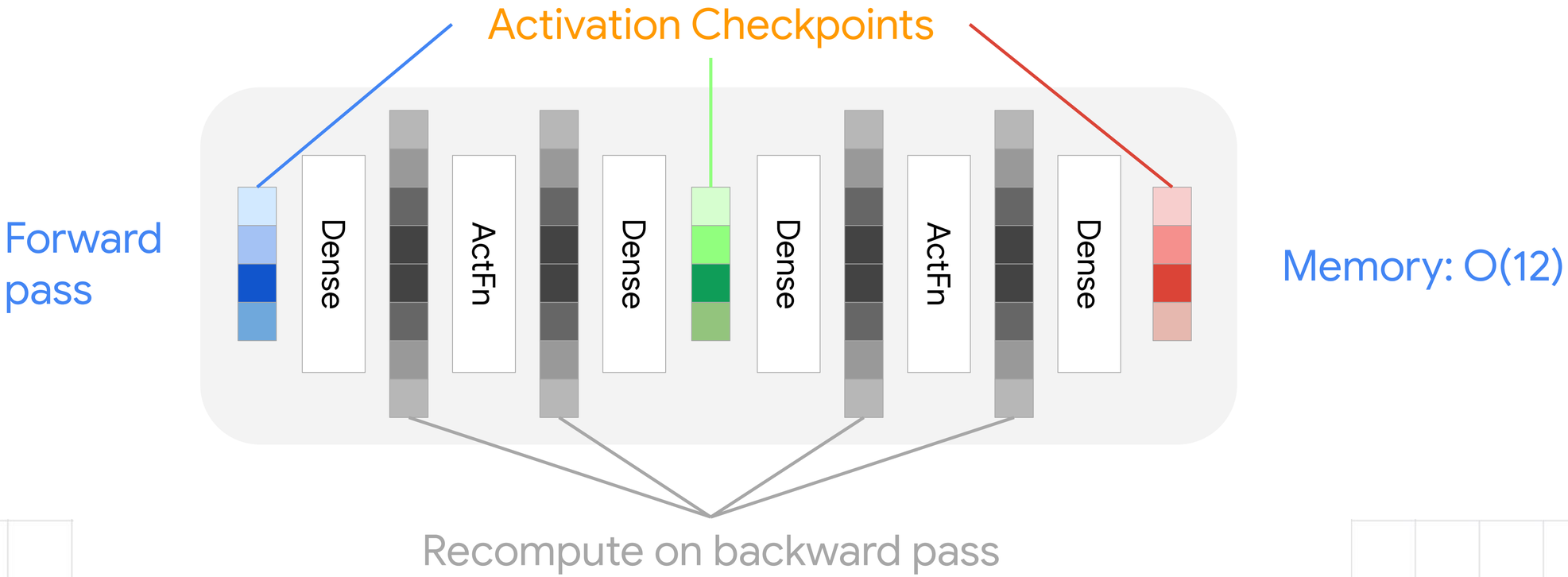
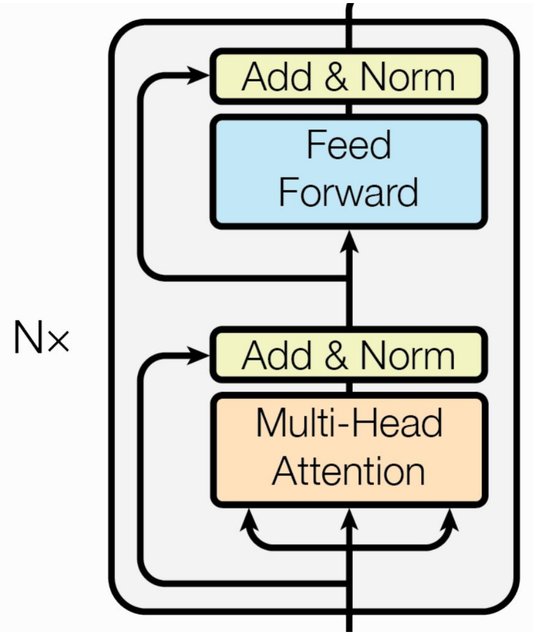
- Alternative: recompute activations on demand



Gradient Checkpointing

- Case study: LLM Transformer (12 layers, 155M)
- Bfloat16 (optimized): 8.8GB memory, 0.7 seconds per step
- Gradient Checkpointing: 3.9GB memory, 0.9 seconds per step
  - **55% memory reduction, 1.25x slow down**
  - Often 90% memory reduction in activations possible
  - Picking the right layers to checkpoint/remat is important



PyTorch:

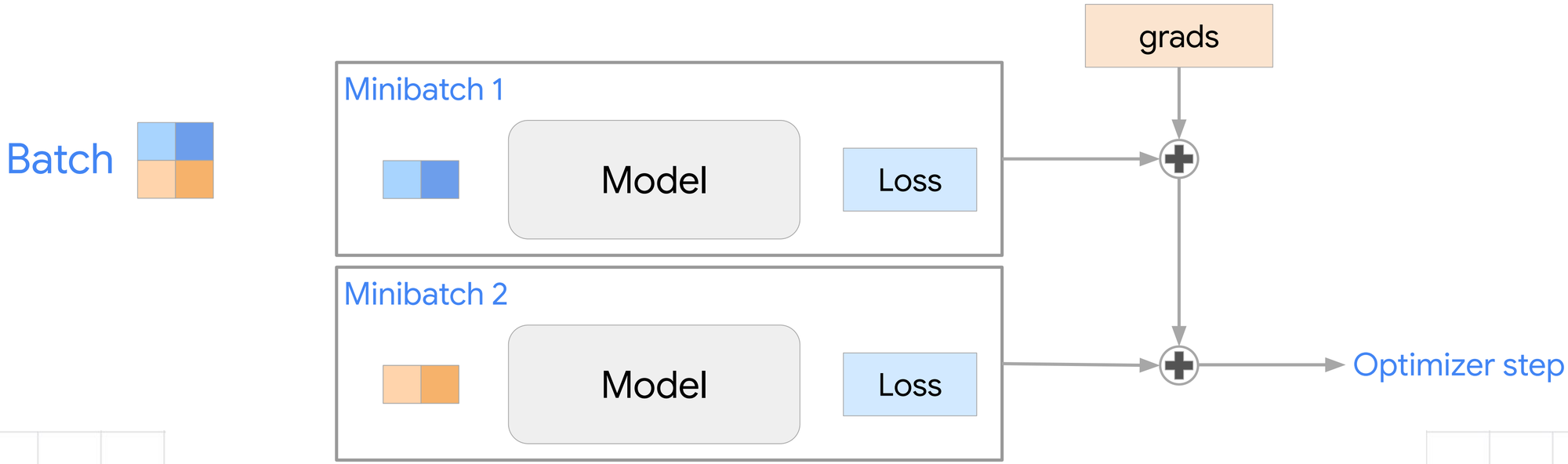
torch.utils.checkpoint (link)

JAX/Flax:

- jax.remat (link)
- flax.nn.remat (link)

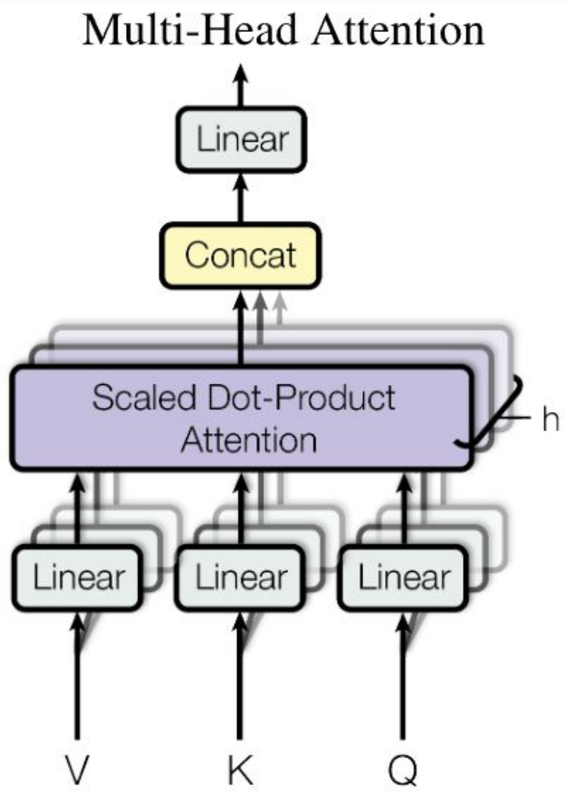
Gradient Accumulation

- Large-model optimizations often require large batch sizes
- Memory only fits small batches
- Idea: accumulate gradients of multiple smaller batches before optimizing



Gradient Accumulation

- Case study: LLM Transformer (12 layers, 155M)
- Gradient Accumulation: 3.9GB memory, 0.91 seconds per step
- Single batch: 6.2GB memory, 0.86 seconds per step
  - **40% memory reduction**, **1.06x slow down**
  - Simple to implement
  - Not always possible to fully utilize the accelerator



CPU Offloading

- If model parameters are larger than GPU HBM, can offload into CPU RAM
  - Also for optimizer parameters
- Load layers one-by-one as needed
- Very slow transfer speed, only as final gamble if nothing else works

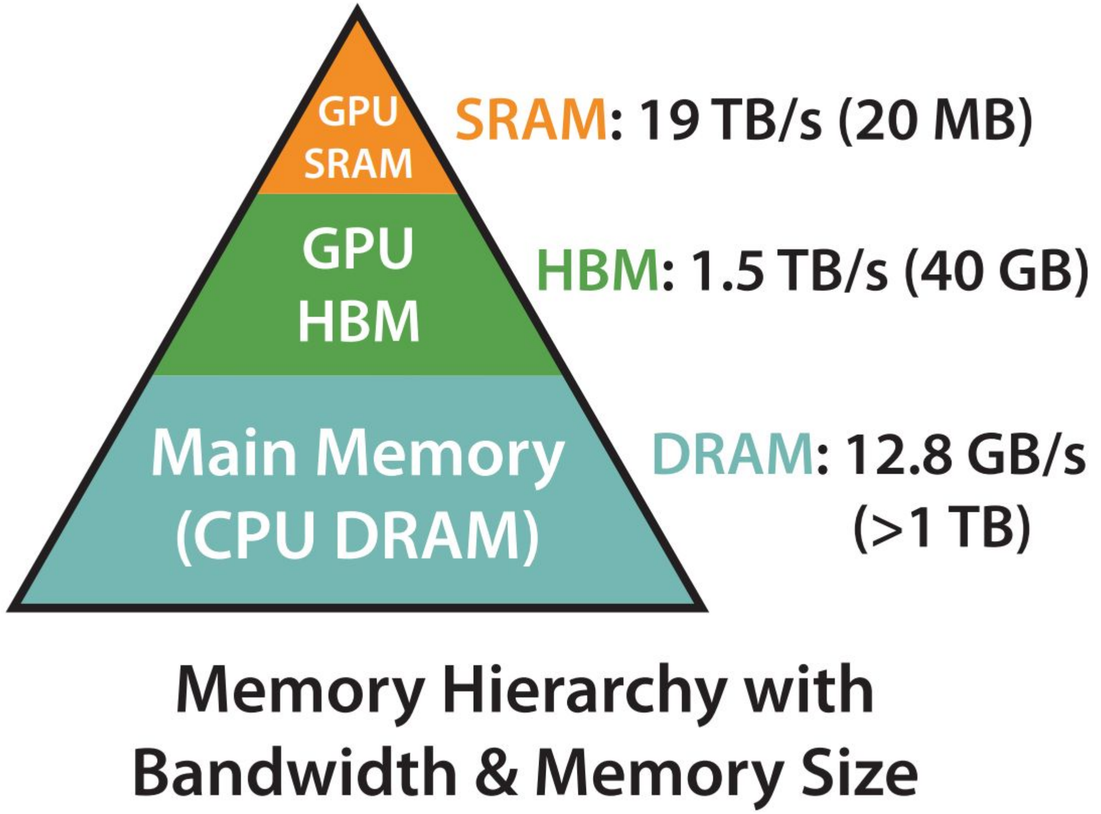


Figure credit: Dao et al., 2022

Profiling

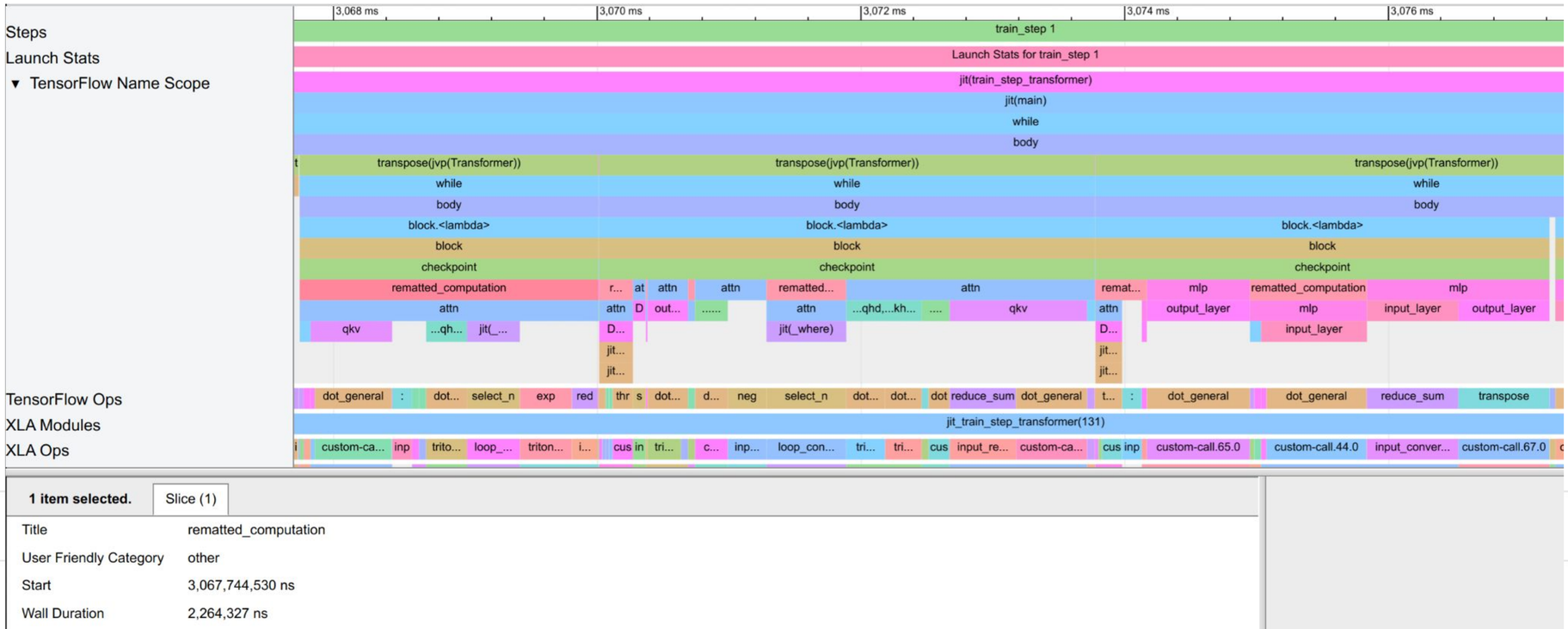
- Crucial to understand the execution of your model
  - Find bottlenecks, memory limitations, “silent” bugs, etc.
- Profiling model execution

PyTorch:

torch.profiler.profile (link)

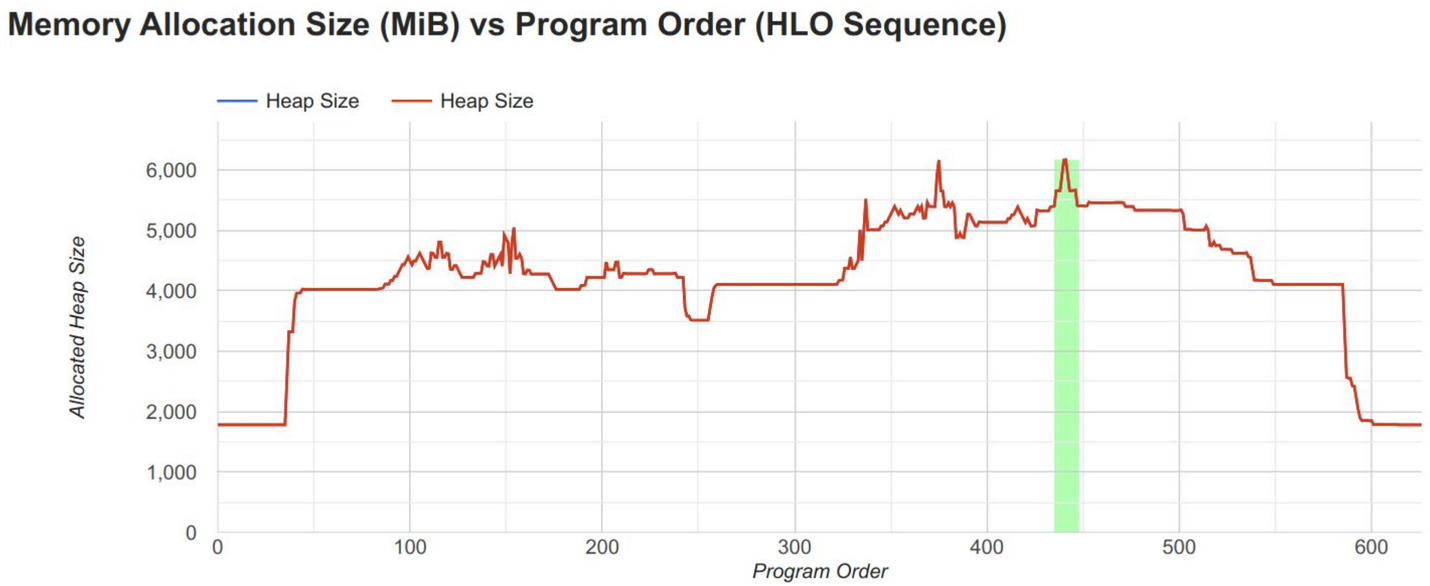
JAX:

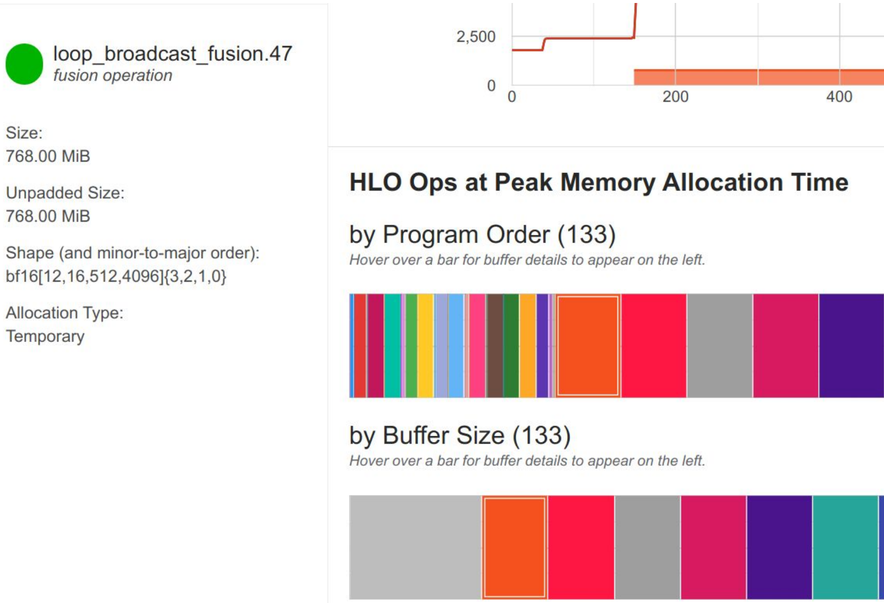
jax.profiler.start_trace (link)



Profiling

- Memory profiling
  - Biggest tensors, when created/free'd, check precision, etc.





Tutorial: [How to read the profile]

Per-Device Optimizations

Summary

Speed-Ups

- Compilation
- Mixed Precision
- Optimized kernels

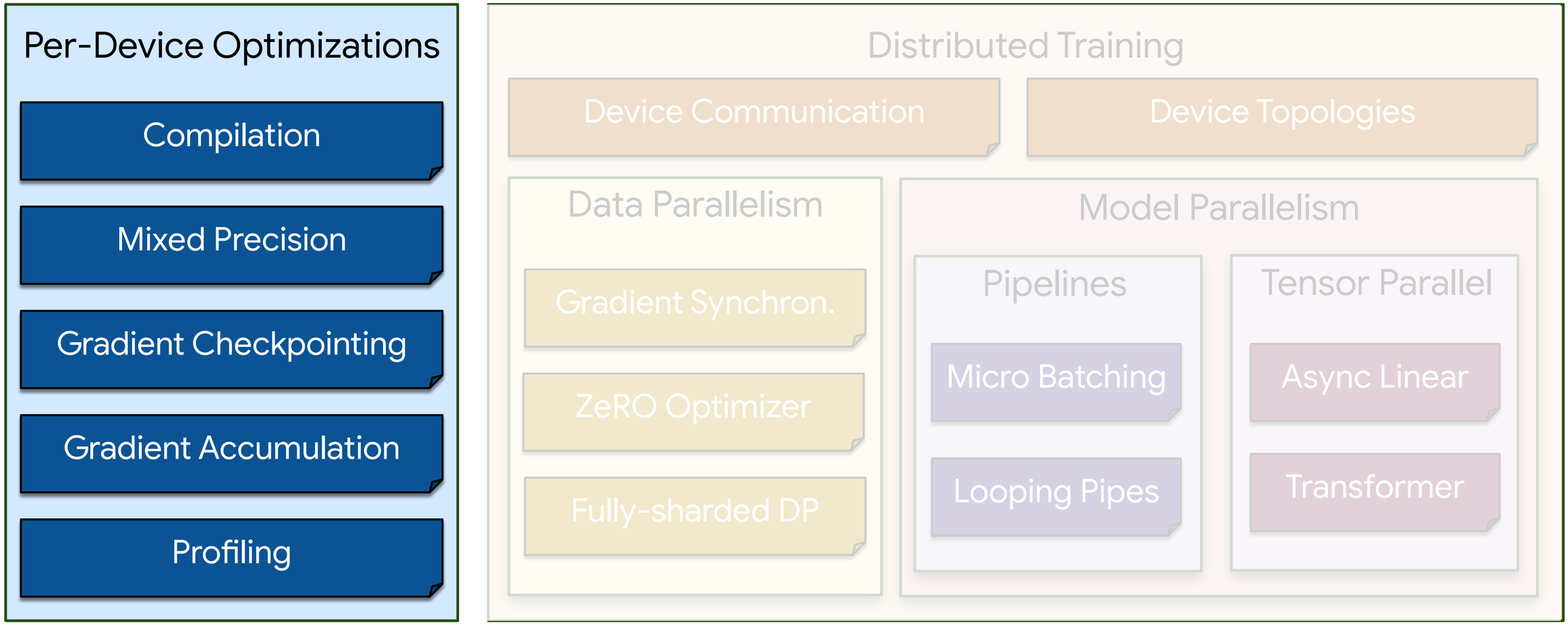
Memory Reduction

- Compilation
- Mixed Precision
- Gradient Checkpointing
- Gradient Accumulation
- CPU Offloading
- Lighter Optimizers

Model Inspection

- Profiling

Overview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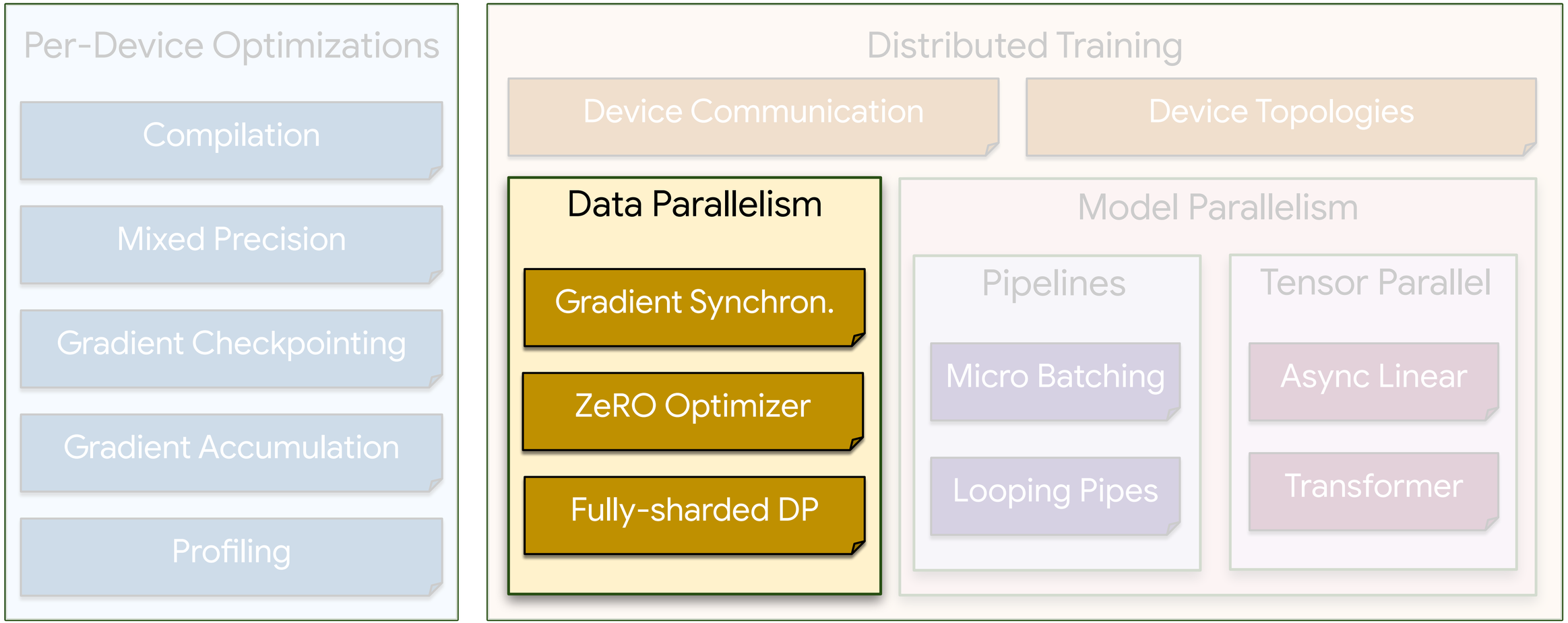
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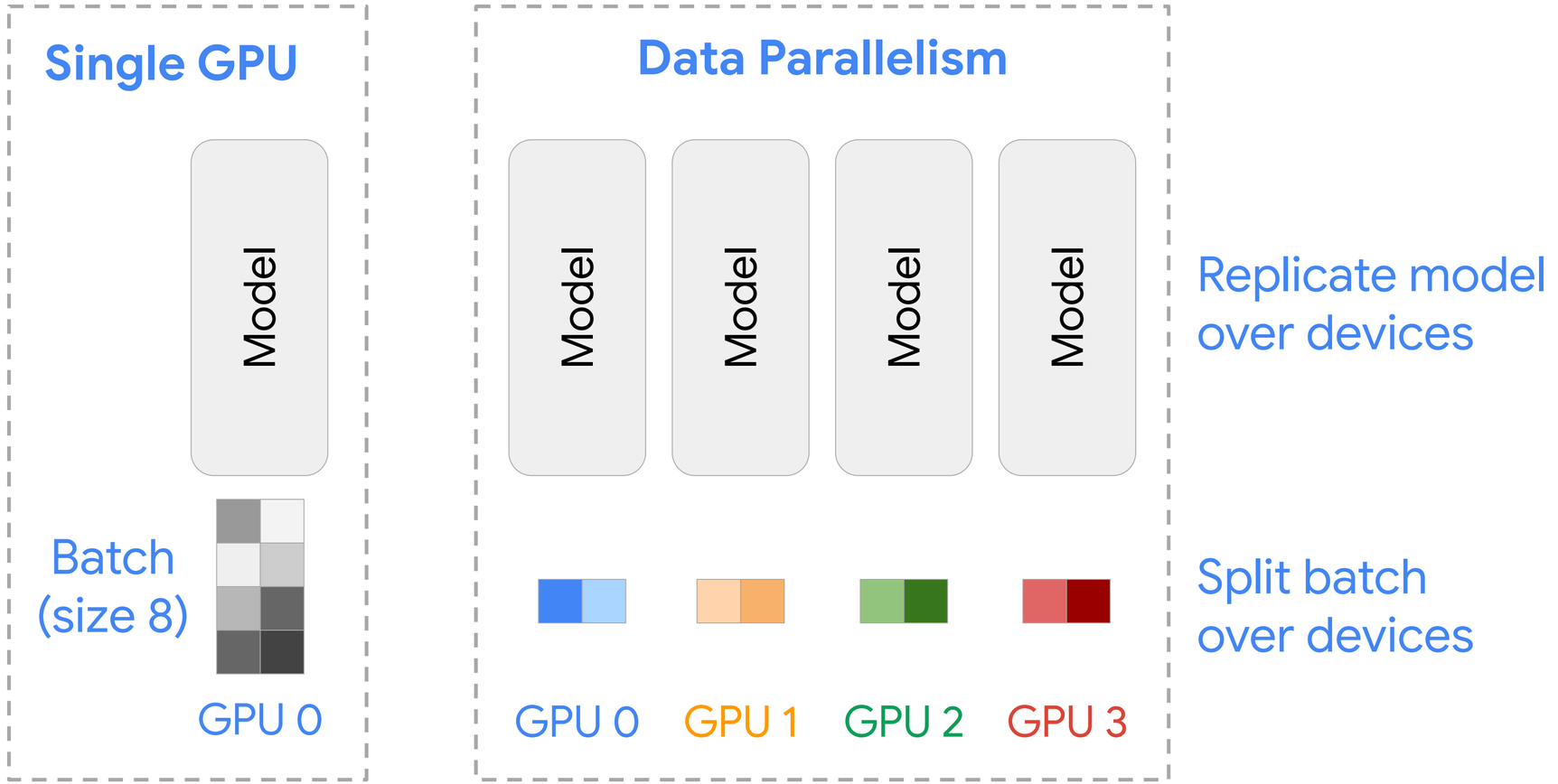
Data Parallelism



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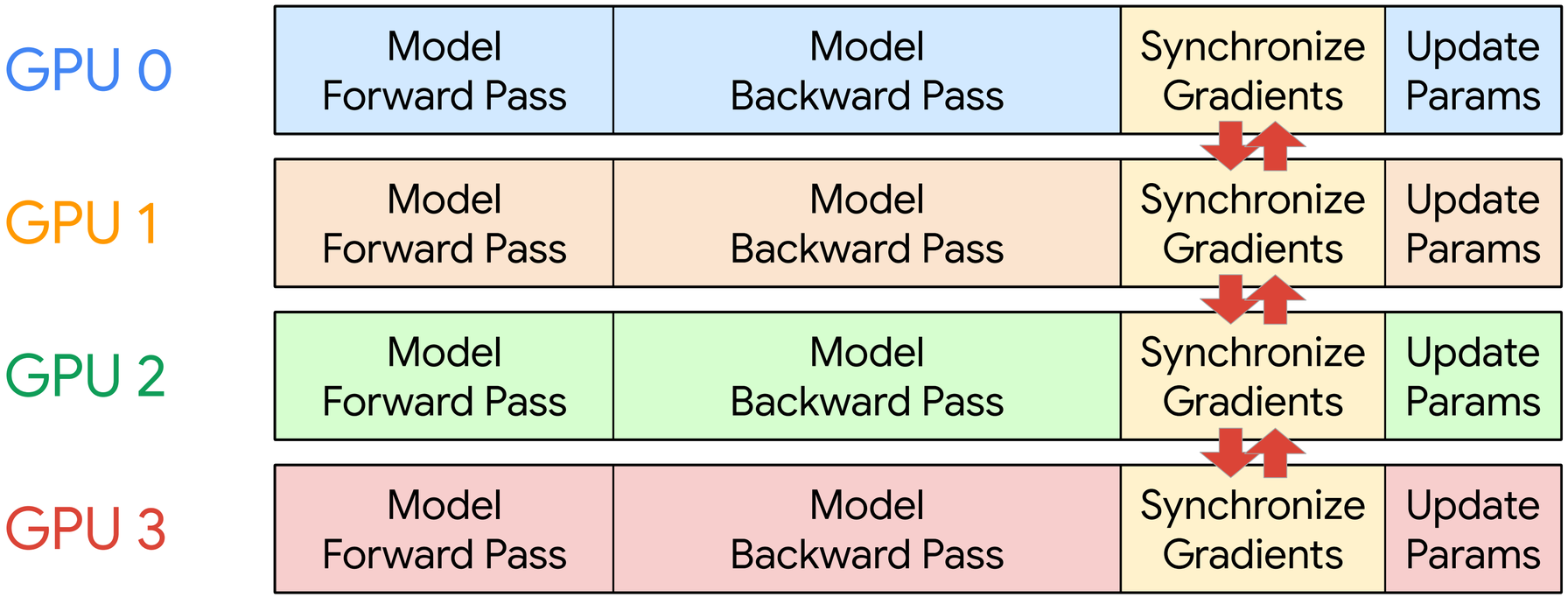
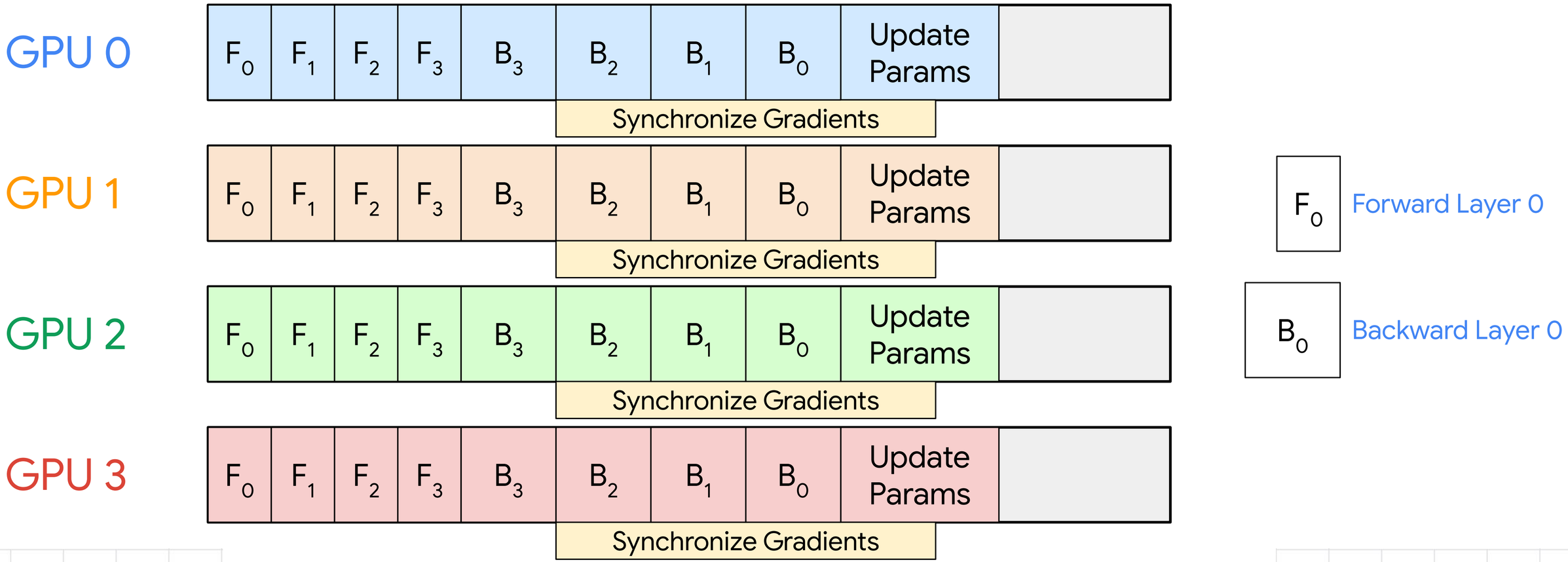


Data Parallelism

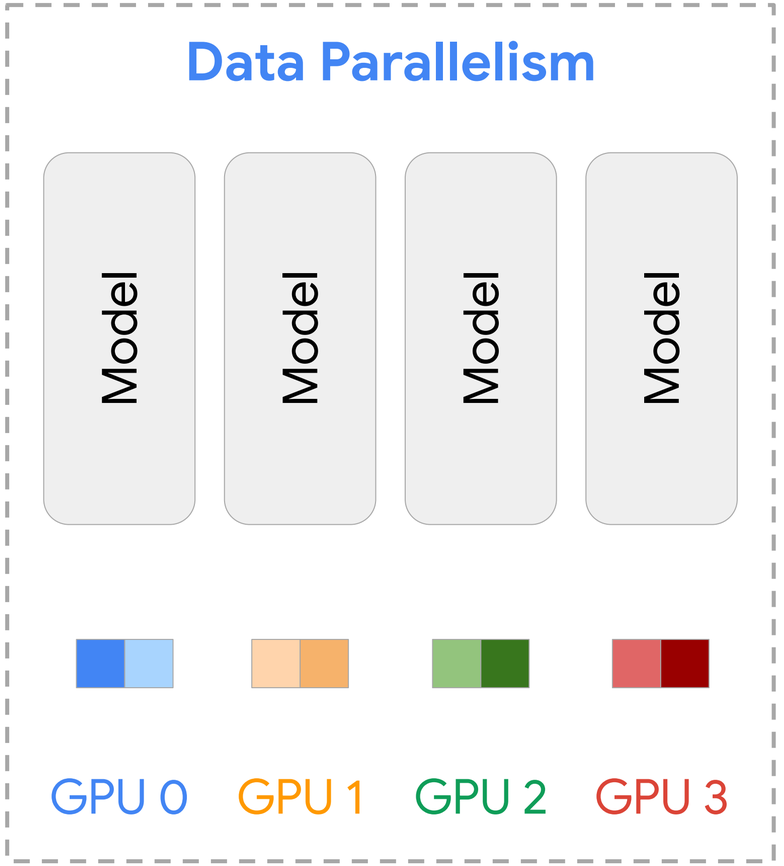
Asynchronous Communication



Data Parallelism

Sharding

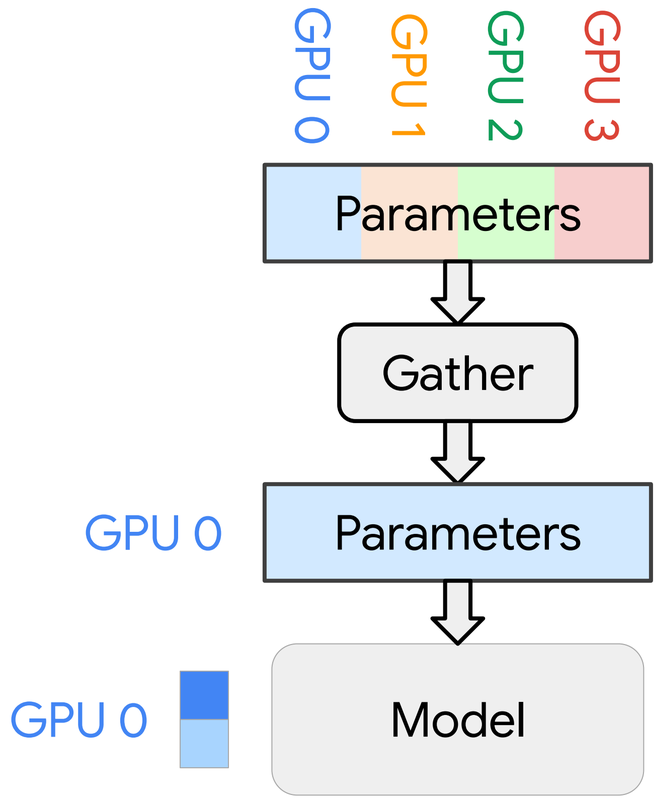
- At 1 billion parameters, replicating model is expensive
  - 16 bytes per parameter ⇒ 16GB on each device



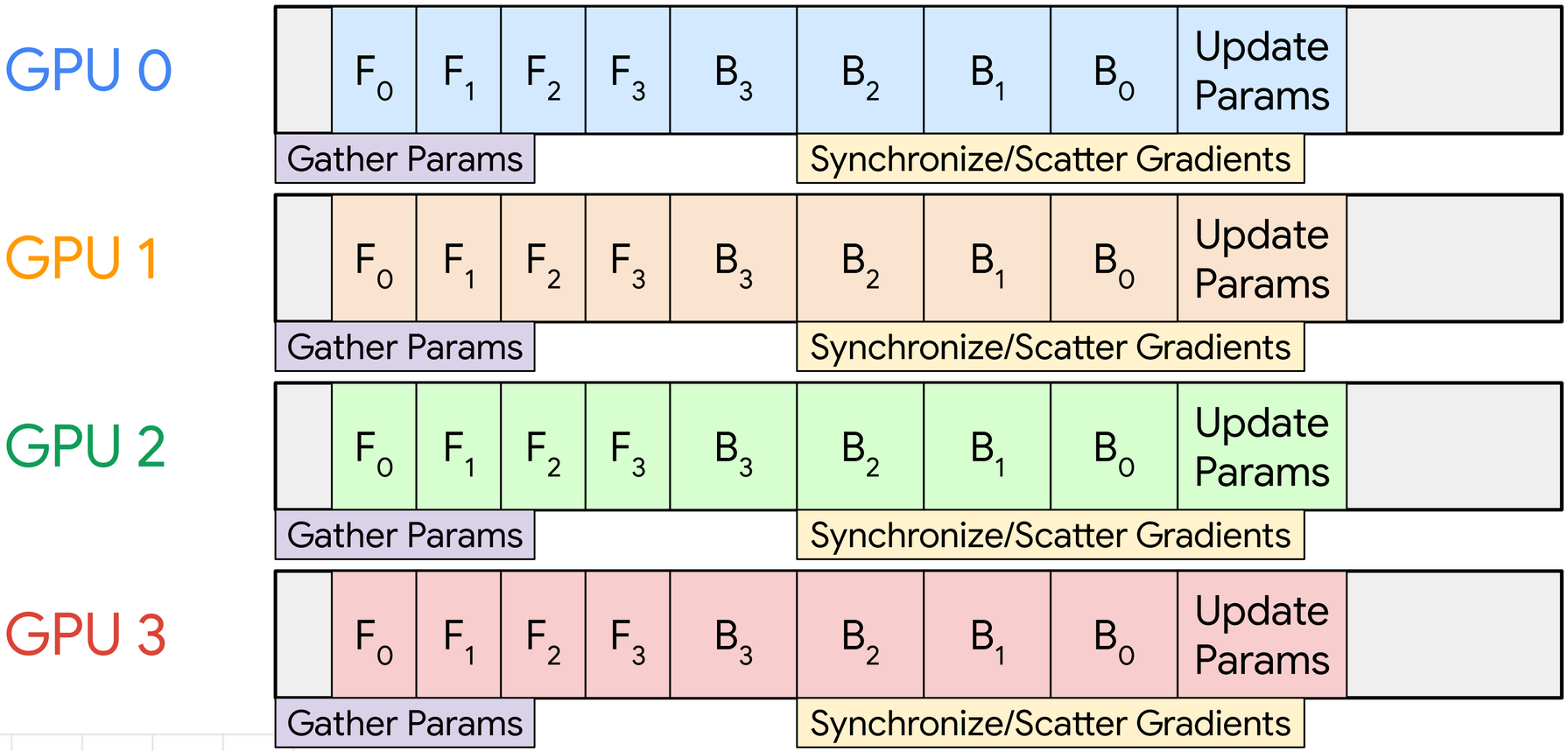
Data Parallelism

Sharding

- At 1 billion parameters, replicating model is expensive
  - 16 bytes per parameter ⇒ 16GB on each device
- Solution: fully-sharded data parallelism
  - Each device holds a part of the model parameters
  - Before model execution, we gather the parameters and continue as usual

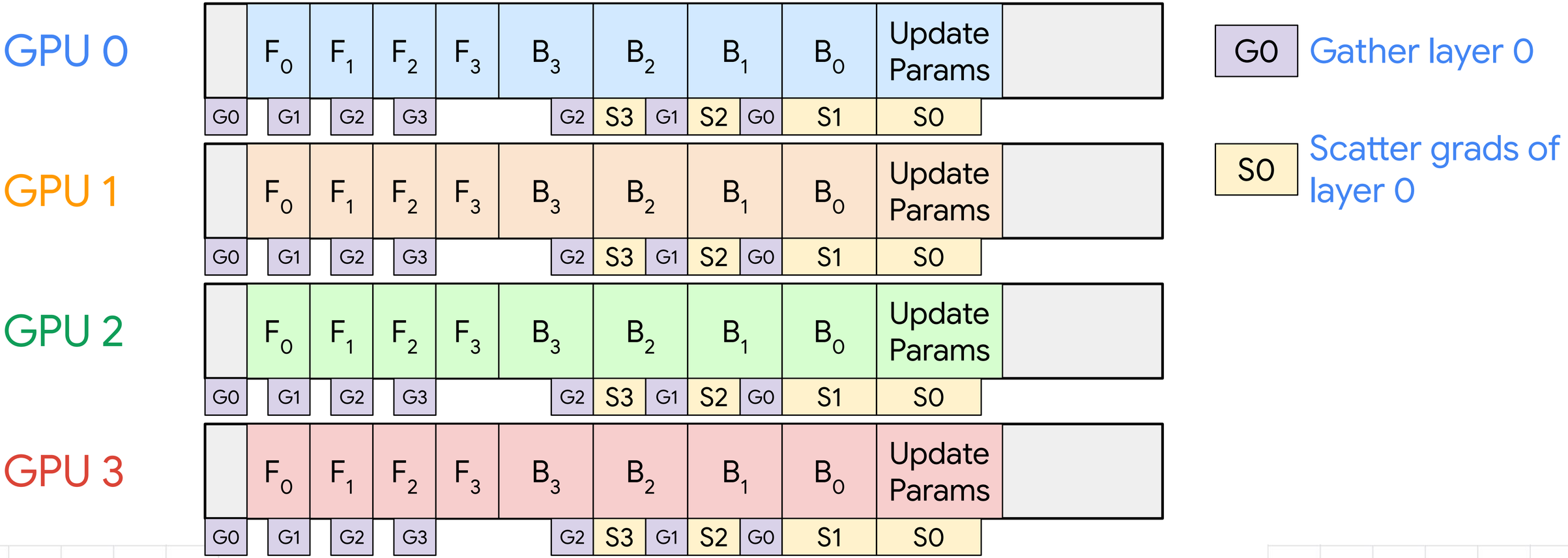


Fully-Sharded Data Parallelism

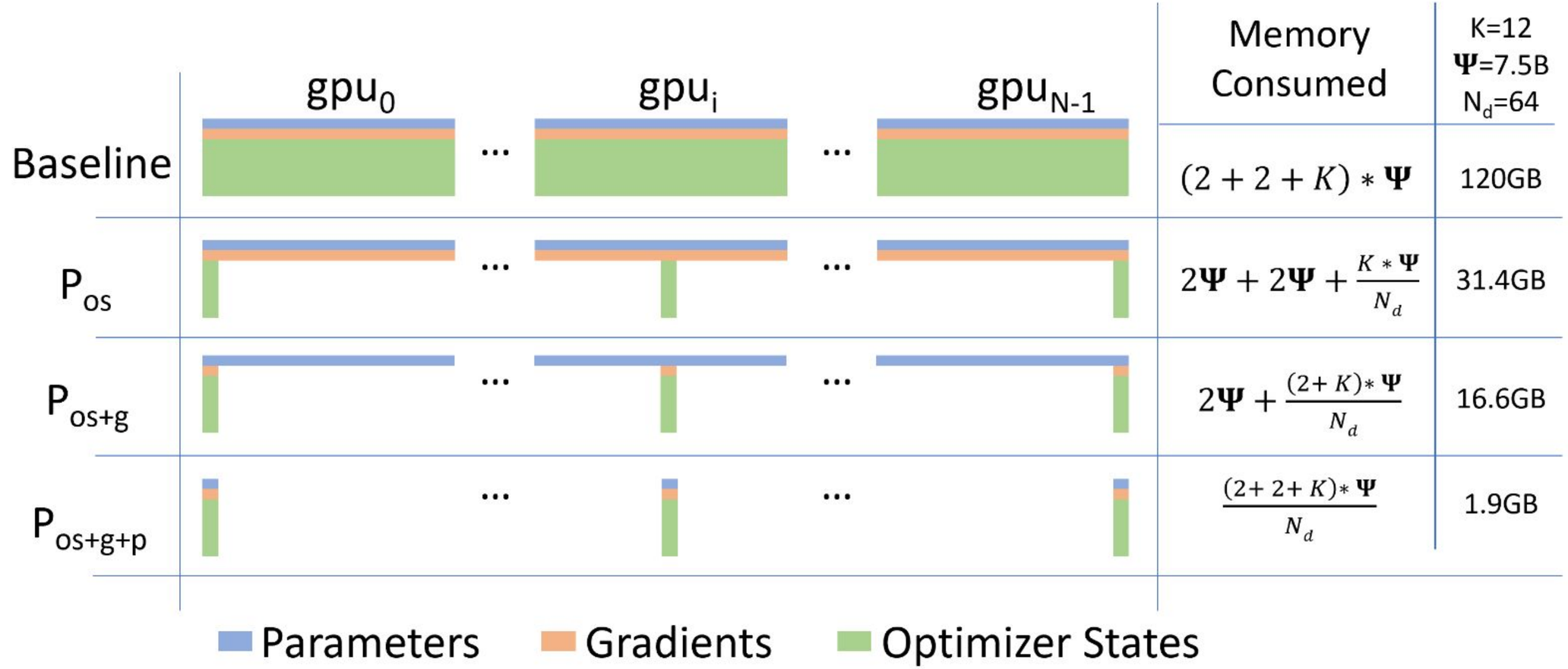


Fully-Sharded Data Parallelism

Gradient Checkpointing



ZeRO Optimizer



Rajbhandari et al., 2019

Data Parallelism

Summary

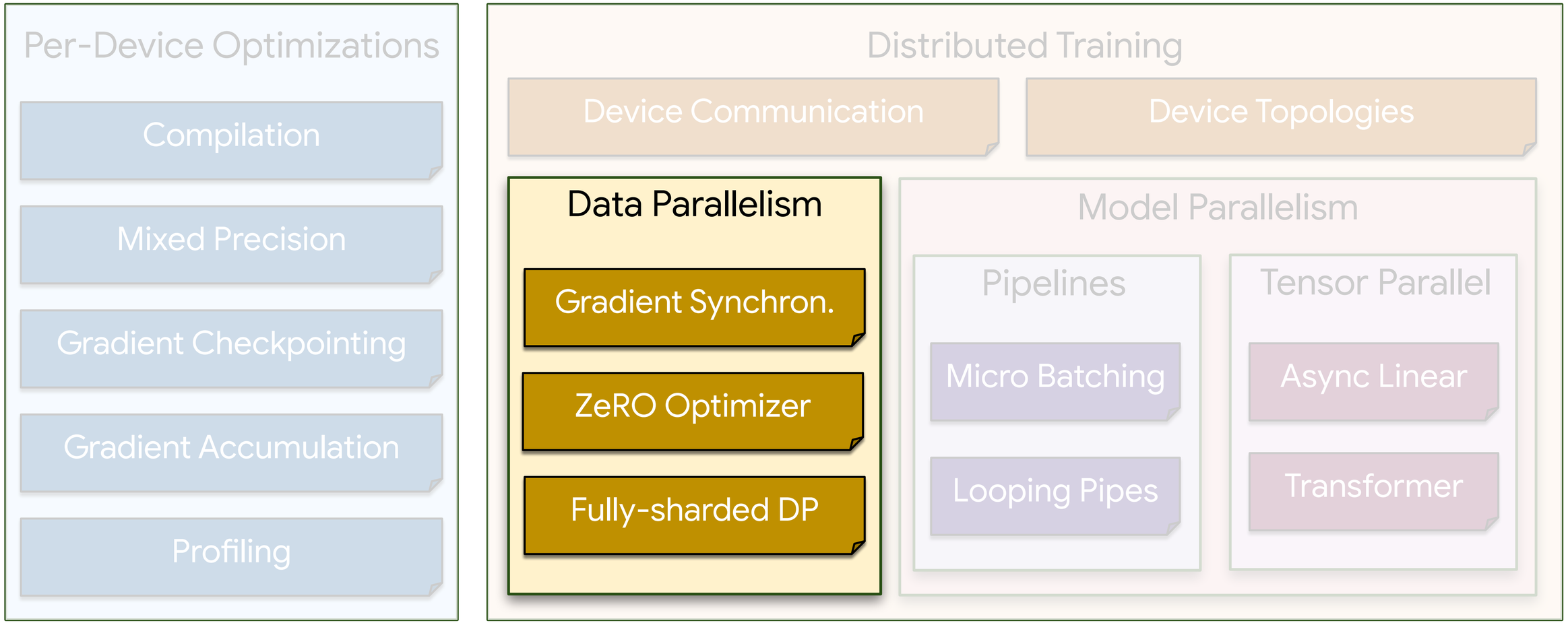
Benefits

- Easy to implement
- Low communication costs
- Parameter sharding reduces memory footprint

Drawbacks

- Each device runs the full model
- Parameter sharding becomes inefficient for slow/large clusters

Overview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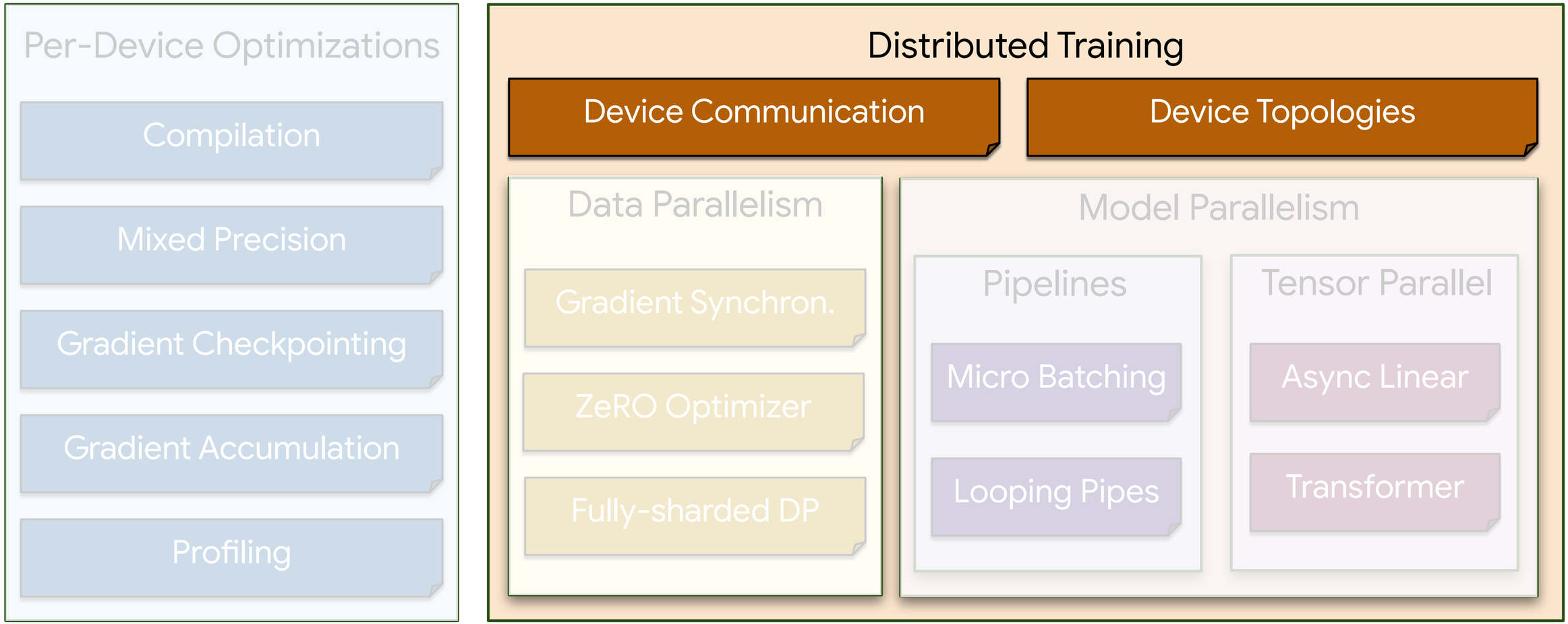
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Device Communications

- Three key communication operations:
  - all_gather
  - reduce_scatter
  - ppermute

There exist more, but we can reduce most of them to these basic blocks

Device Communications

all_gather

- Replicate across devices
- Forward pass FSDP

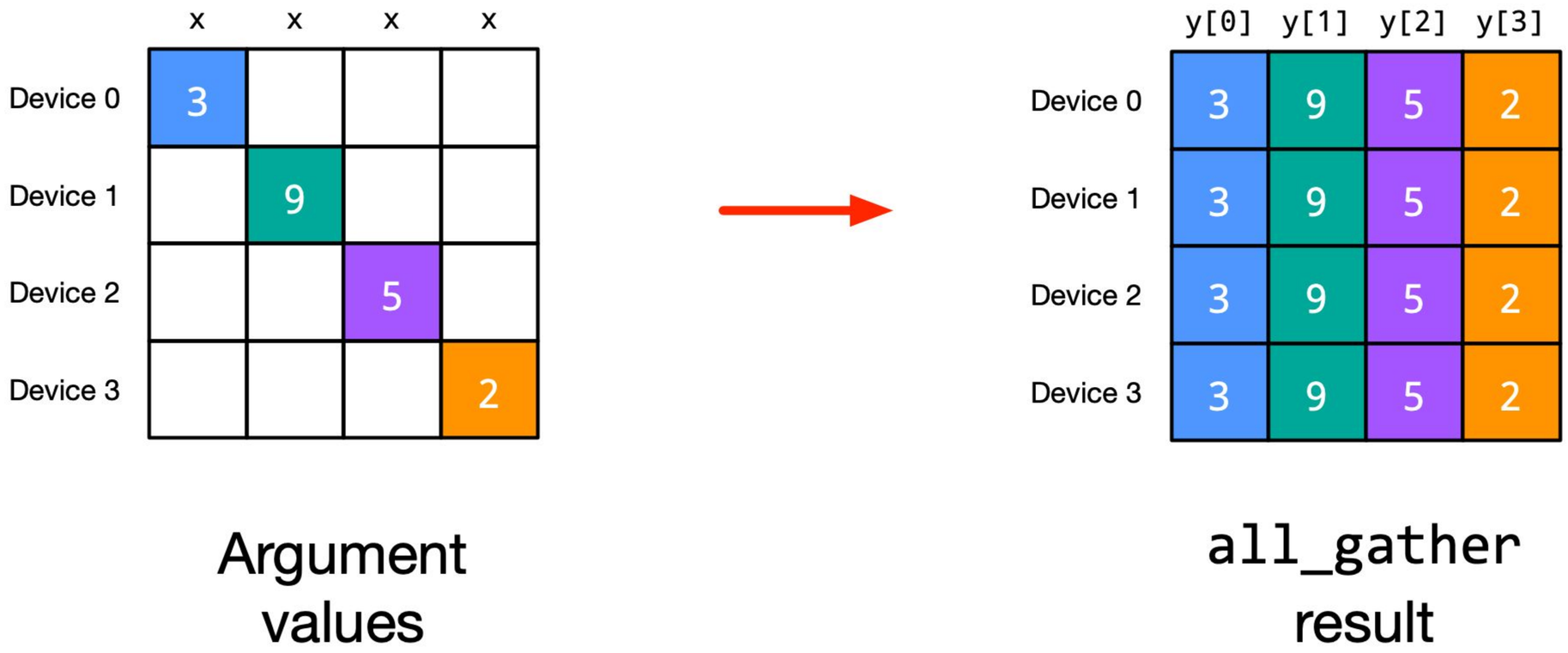


Figure credit: JAX Team

Device Communications

reduce_scatter

- Gradient fn of all_gather
- Backward pass FSDP
- Other reduce ops possible

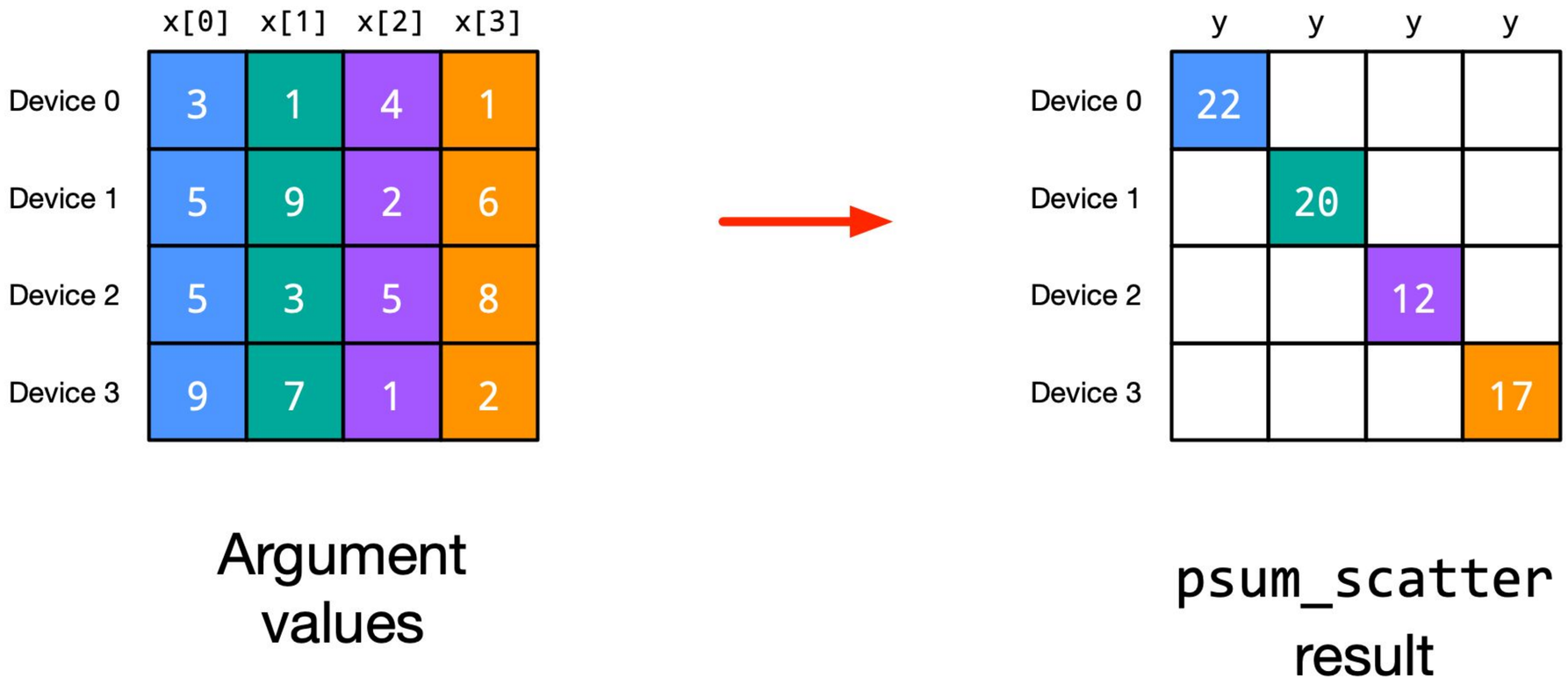


Figure credit: JAX Team

Device Communications

ppermute

- Round-robin communication
- Ideal on a ring
- Can implement other comms. (more later)

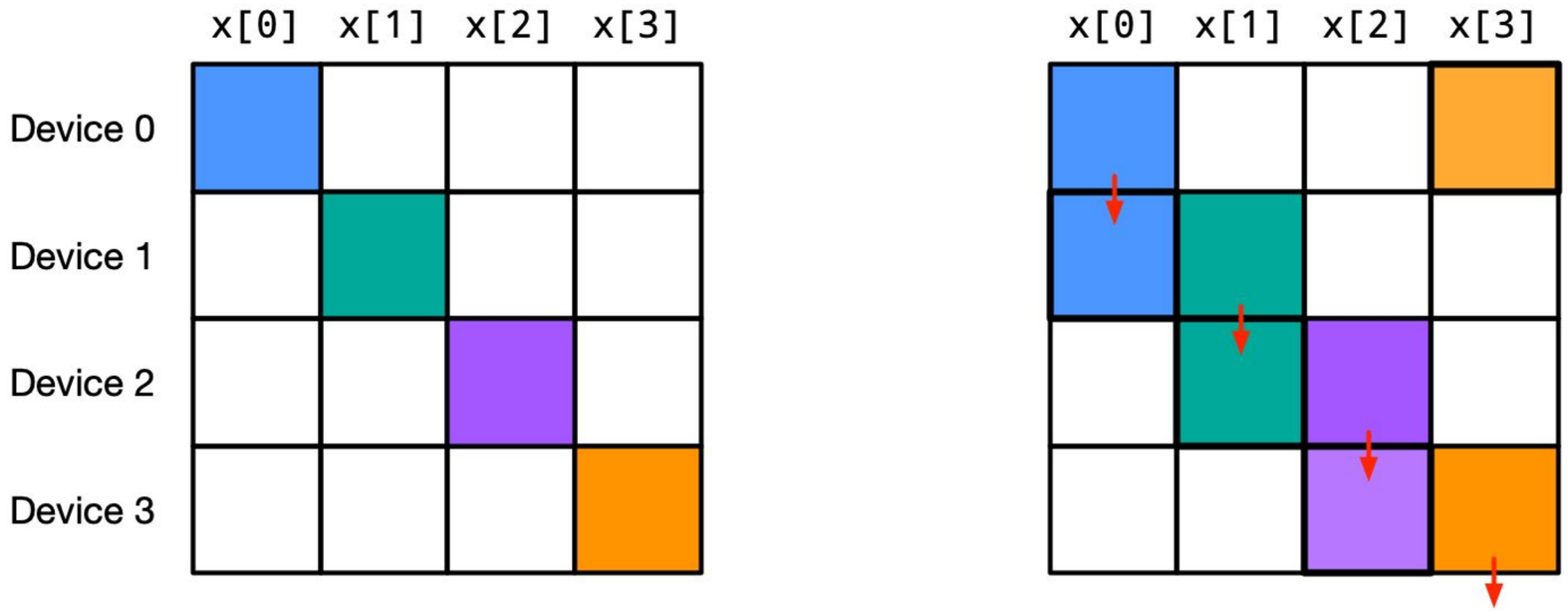
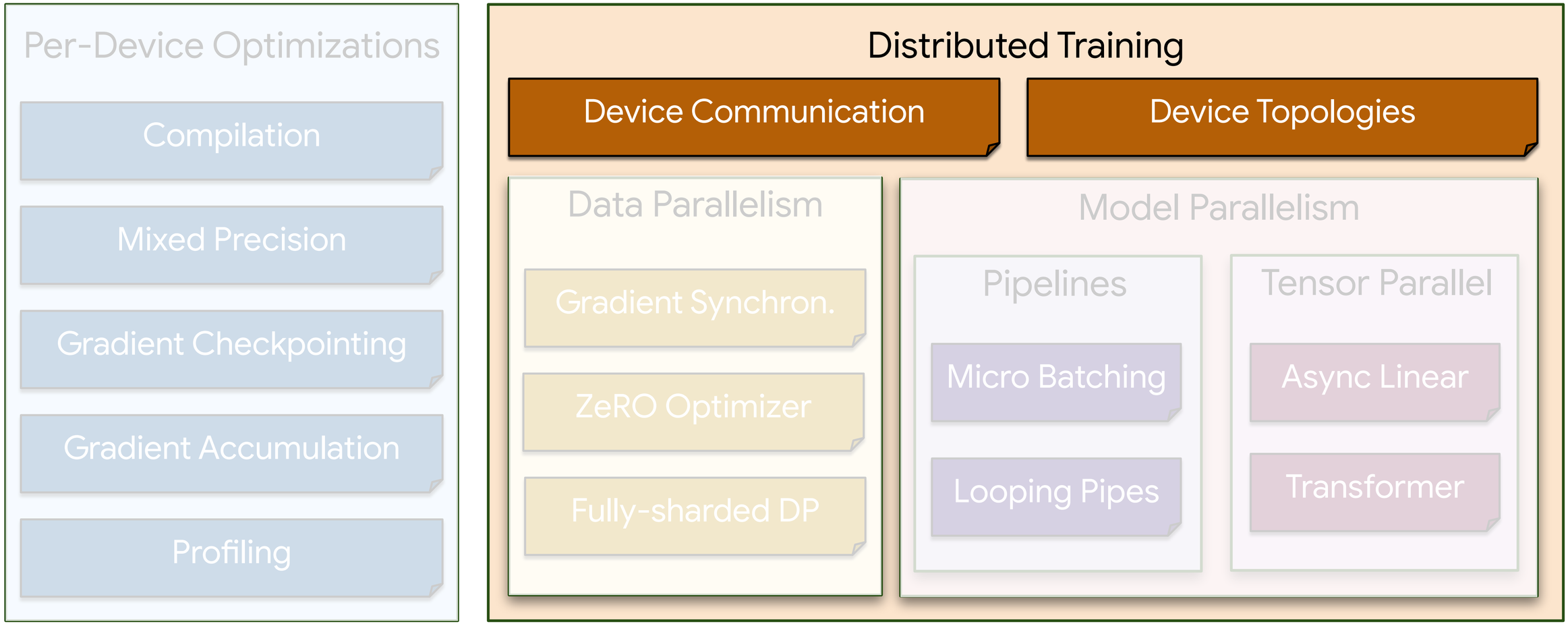


Figure credit: JAX Team

Overview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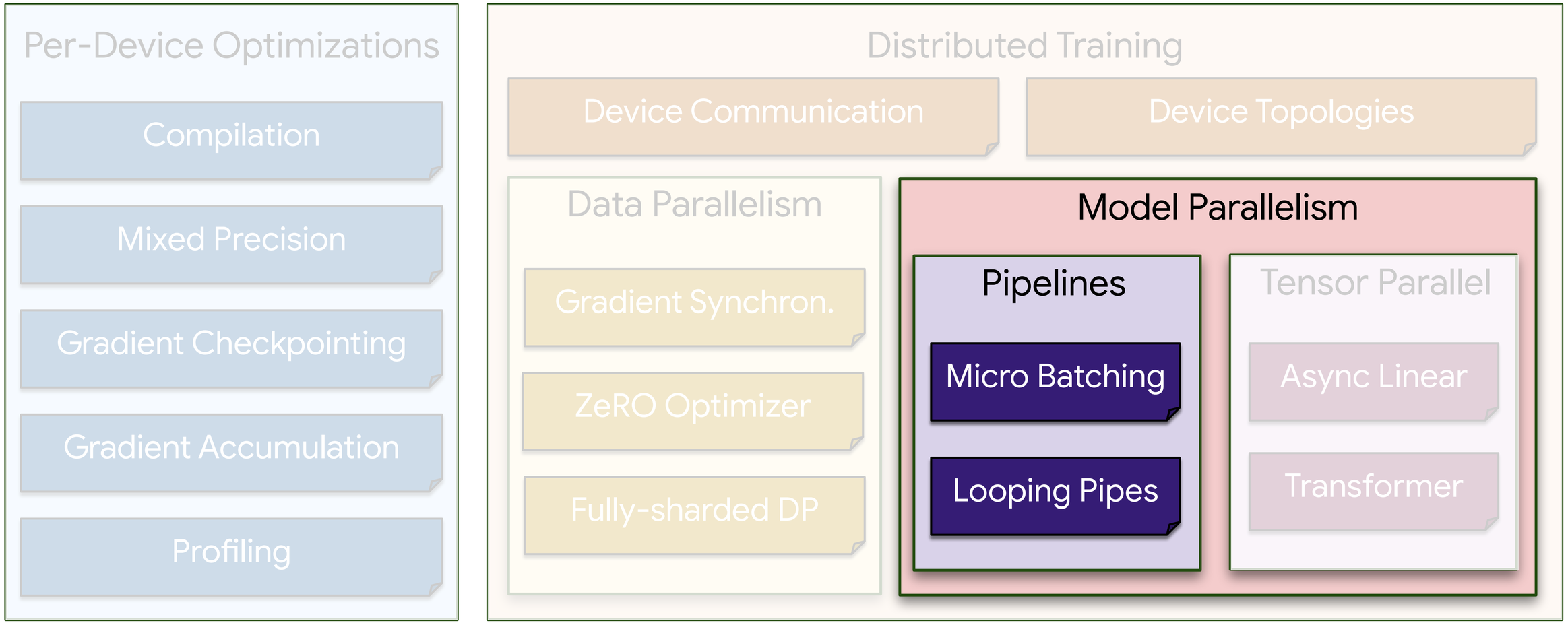
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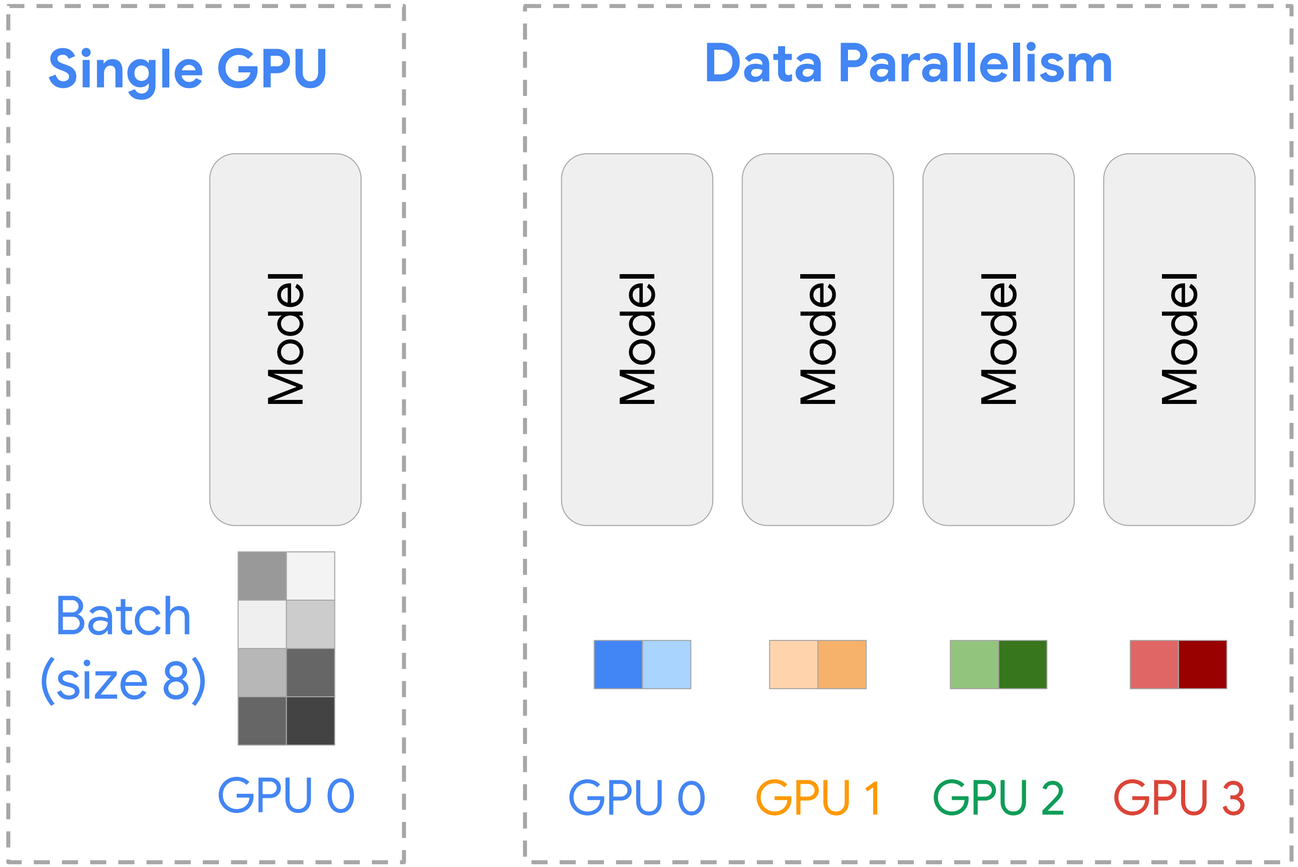
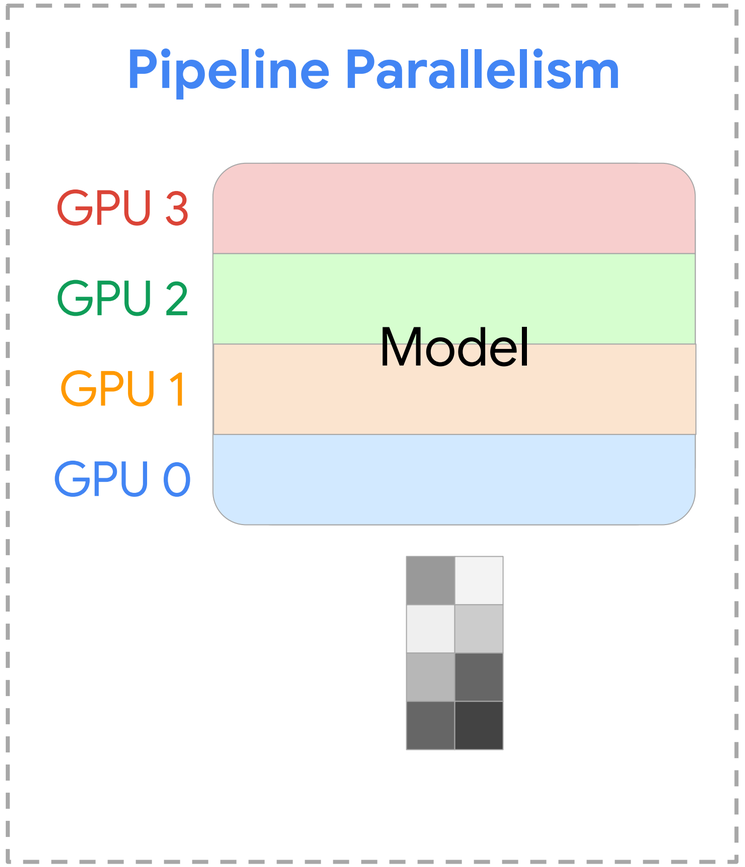
Model Parallelism

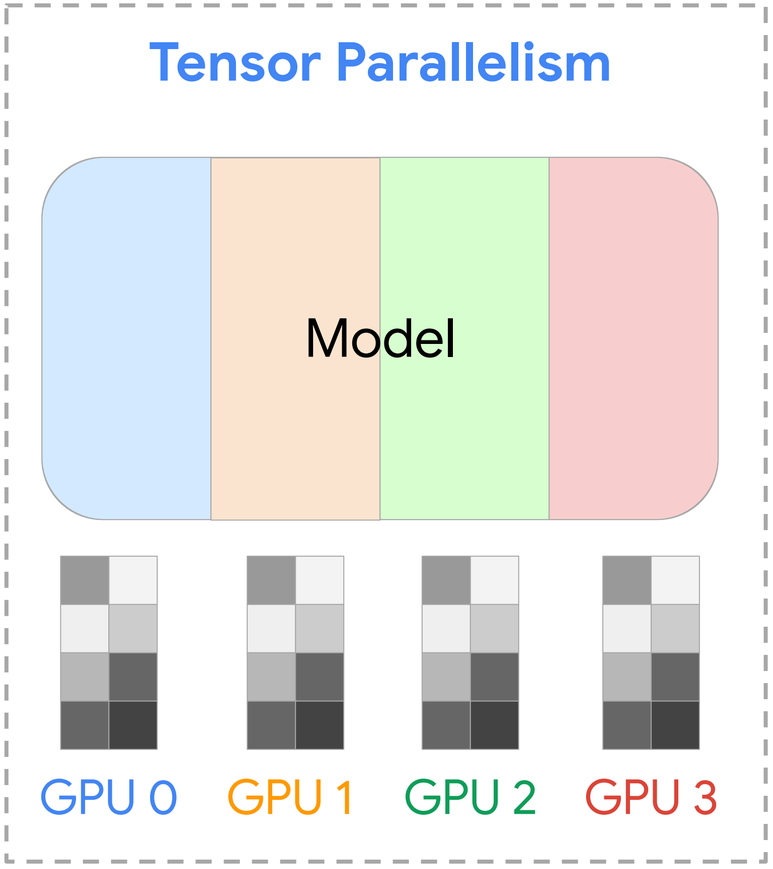
- Fully-sharded data parallelism becomes inefficient over many nodes
  - Slow communication
  - Tiny batch sizes can't achieve max utilization
- Alternative: parallelize the model itself



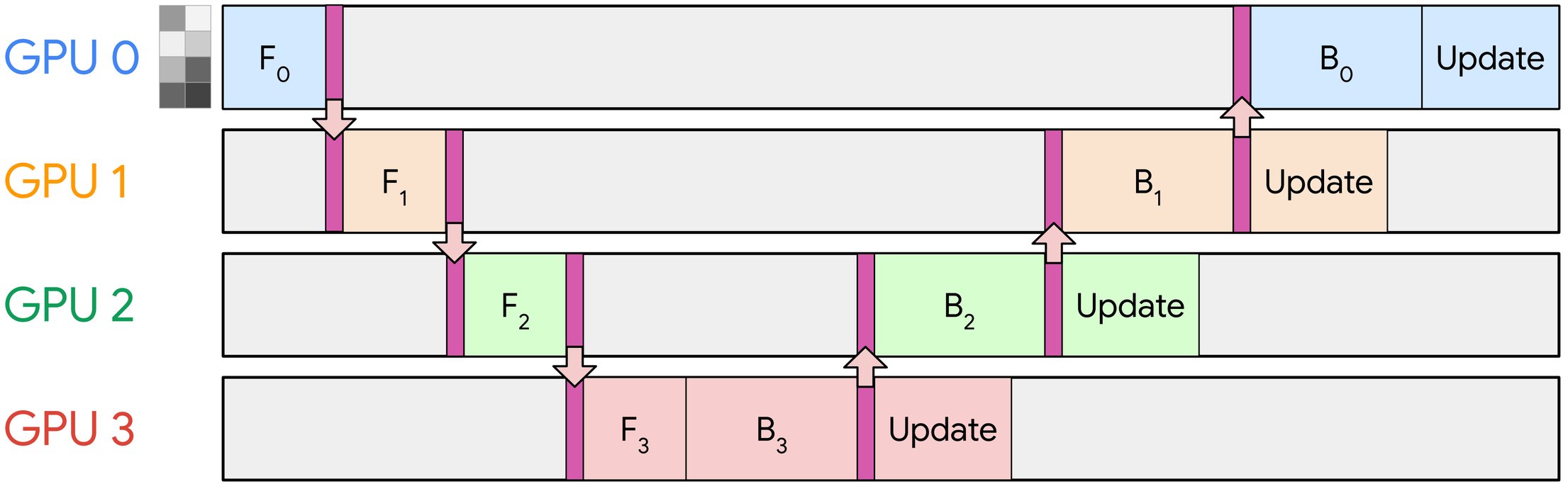
Model Parallelism

- **Pipeline** parallelism distributes over **layers**
- **Tensor** parallelism distributes over **features**





Pipeline Parallelism



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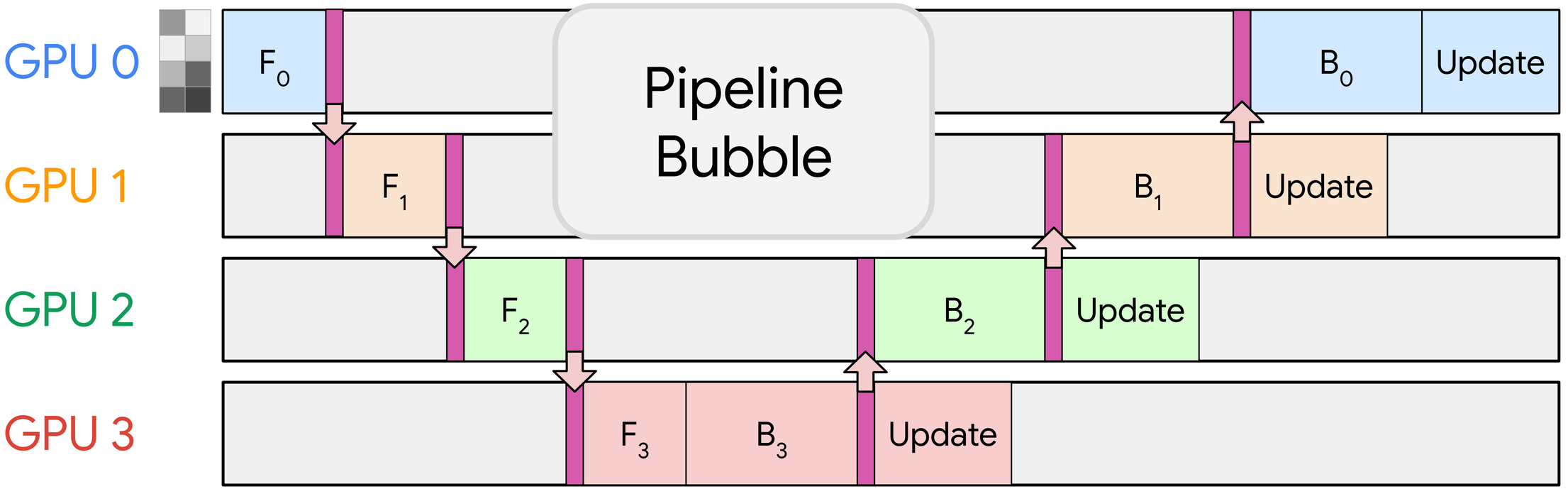
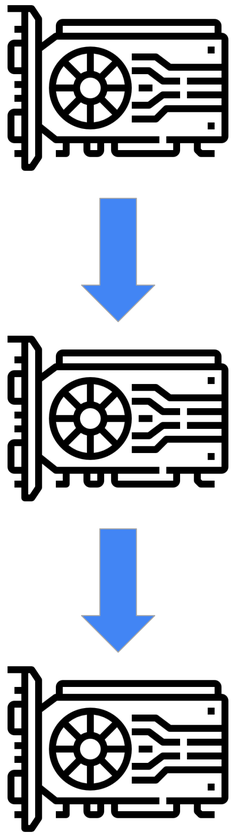


Pipeline Parallelism

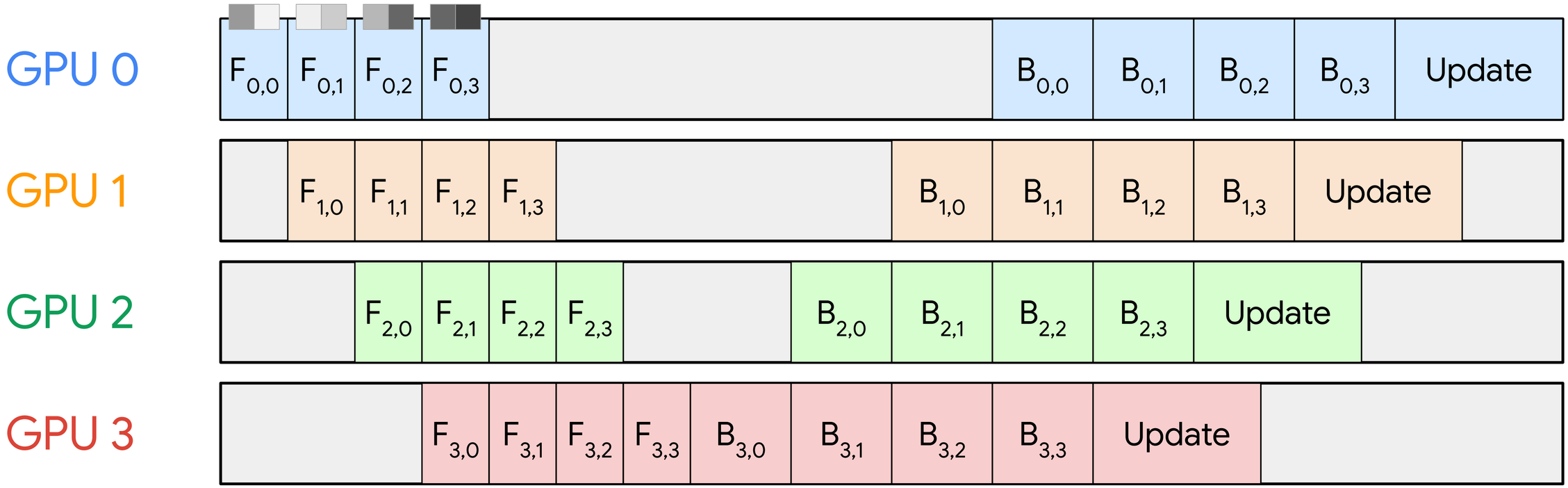
Pipeline Bubble

- Pipelines struggle with keeping devices busy
- Simple idea: Micro-Batching
  - Split batch into multiple smaller batches
  - Run batches one at a time
  - Communicate as soon as one microbatch finishes



Pipeline Parallelism

Micro-Batching



$F_{i,j}$ Forward pass, layer i, micro-batch j

Handcrafted Pipeline Schedules

- More complex schedules for increased speed and memory efficiency
  - Combining with gradient accumulation to free memory of early microbatches
- Increased implementation complexity
- More toolkits out there for [PyTorch]

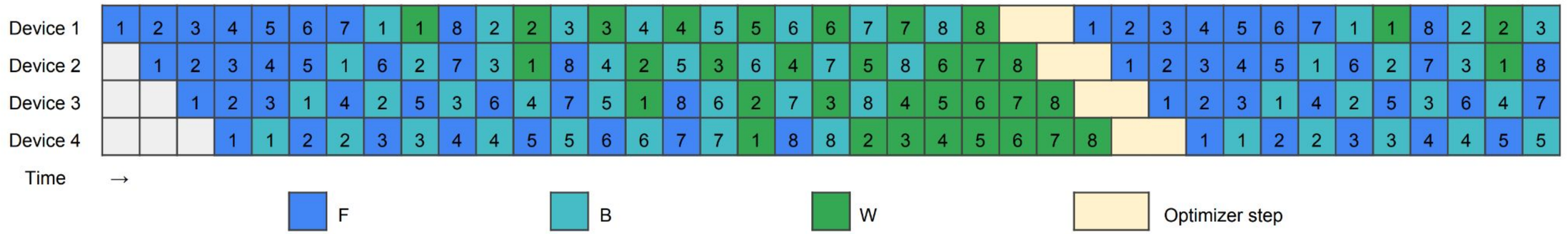
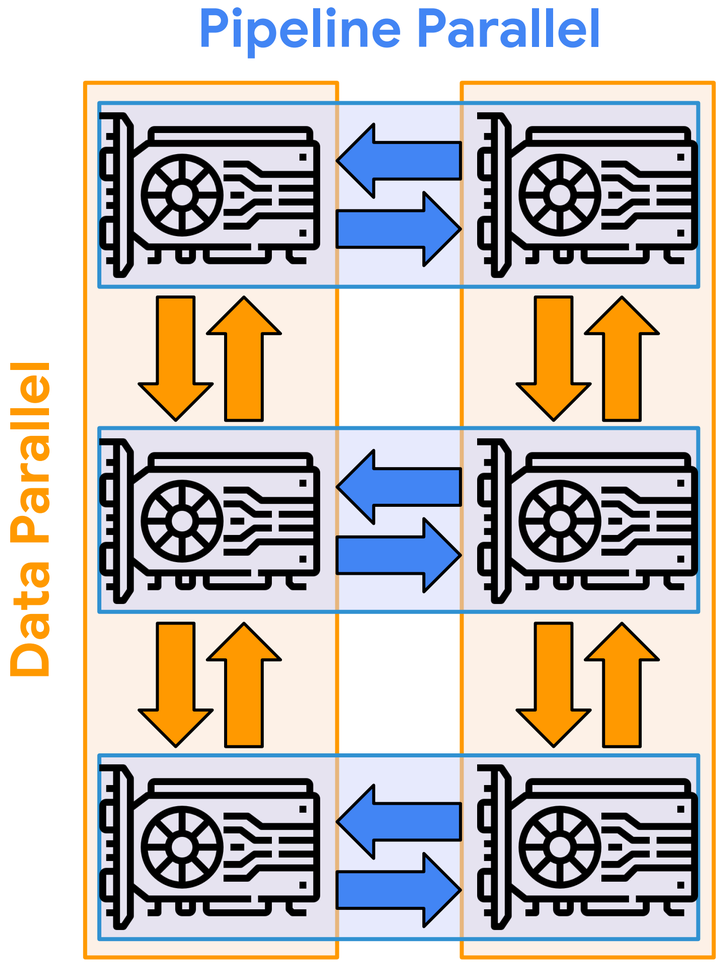


Figure credit: [Qi et al., 2023]

2D Parallelism

- Parallelism strategies complement each other well
  ⇒ combine over device mesh
- Use pipeline parallel over fast connections
  - Allows for larger models
- Use data parallel over slower connections
  - Allows for larger batch size



Pipeline Parallelism

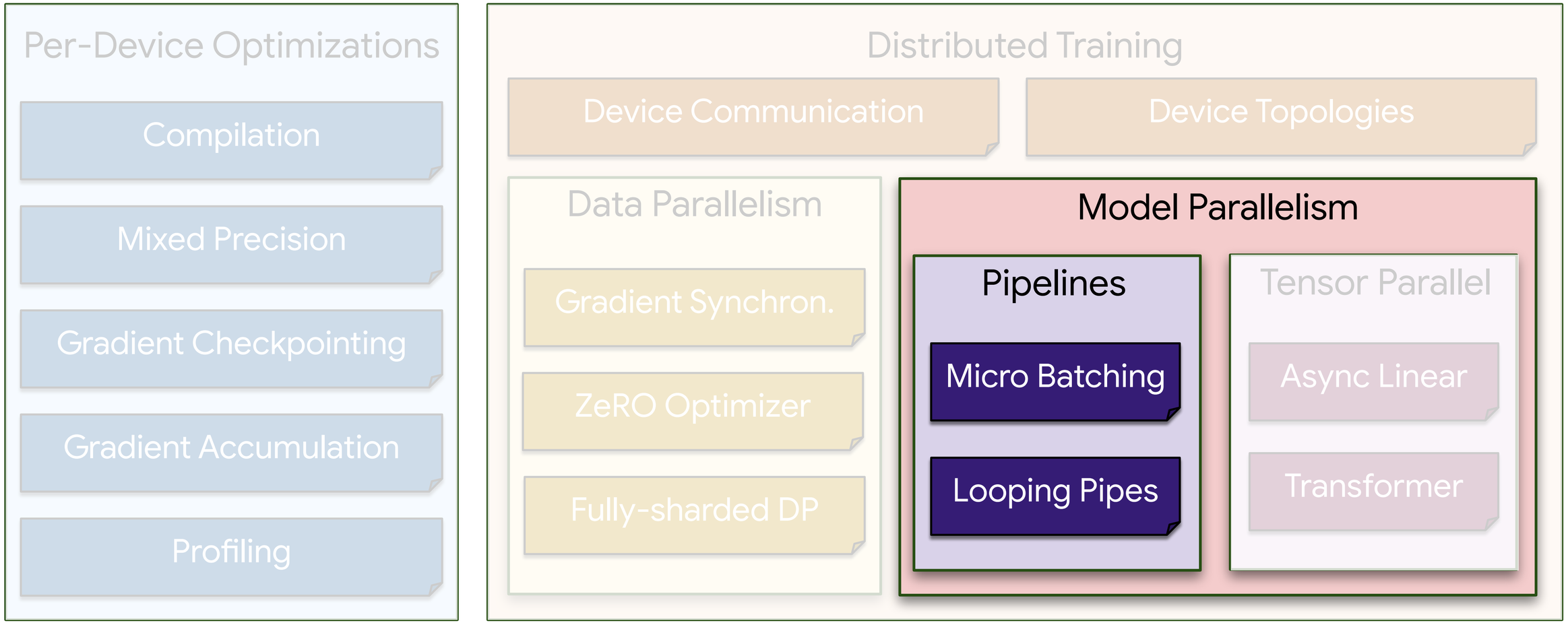
Benefits

- Scales to extremely large models
- Only few communications per execution needed
- Can be generally adapted to any DL model

Drawbacks

- Pipeline bubble reduces efficiency
- Requires many micro-batches
- Communication non-async
- Complex handcrafted schedules

Overview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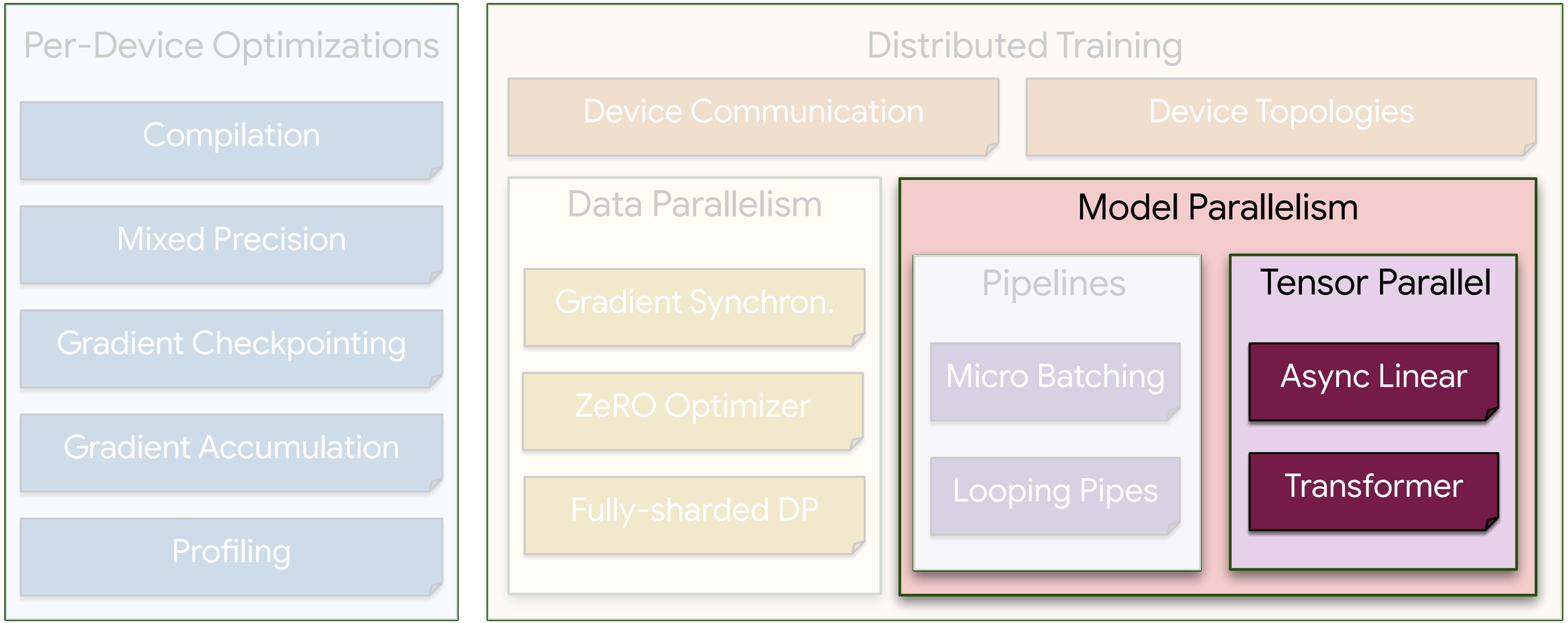
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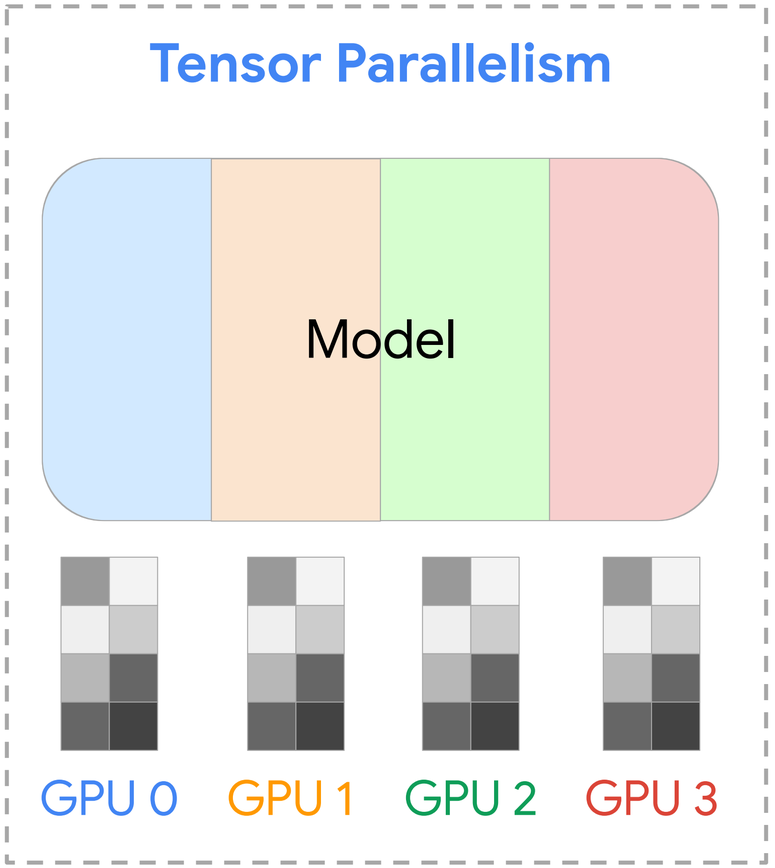
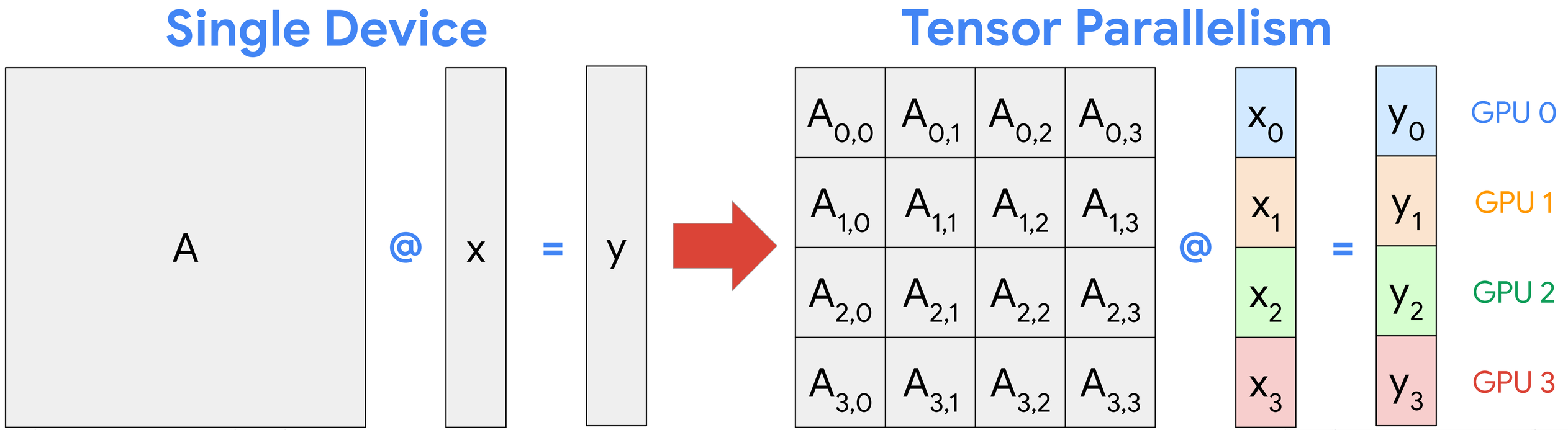
Tensor Parallelism

- **Tensor** parallelism distributes over **features**
- Each layer will be distributed over multiple devices
- Key technology behind ViT-22b, Megatron-LM, OPT-175b, and more transformer-based models



Tensor Parallelism

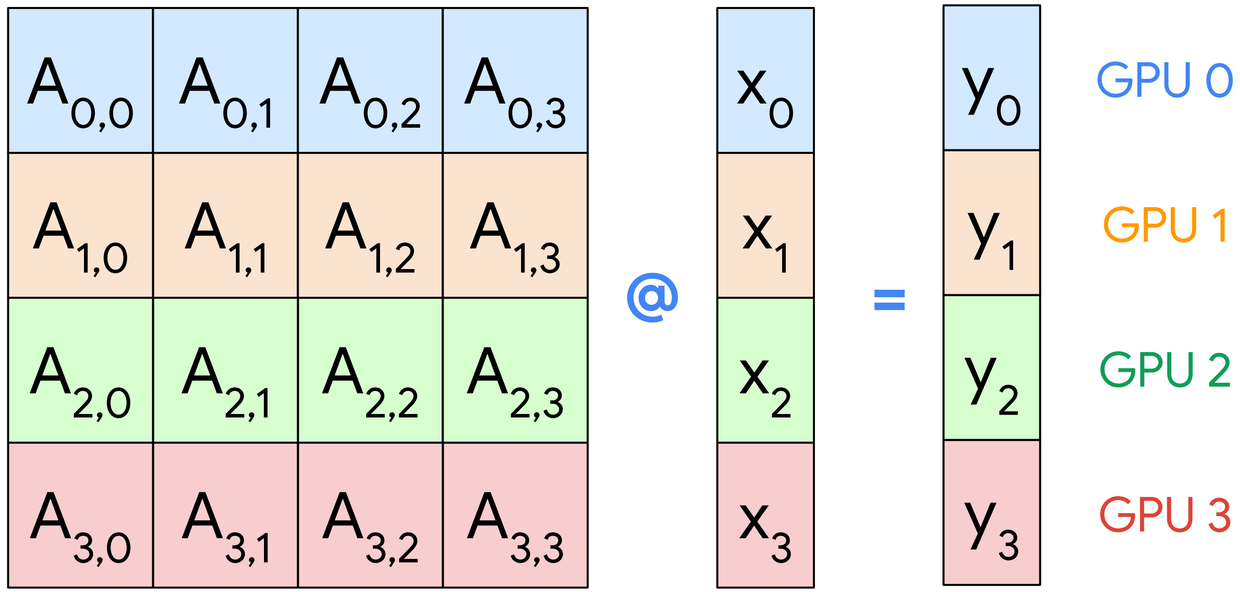
Linear Layer



Tensor Parallelism

Linear Layer - Gather

- First, each device **gathers** the features from all devices
- Matmul with device-own parameters gives device-own output



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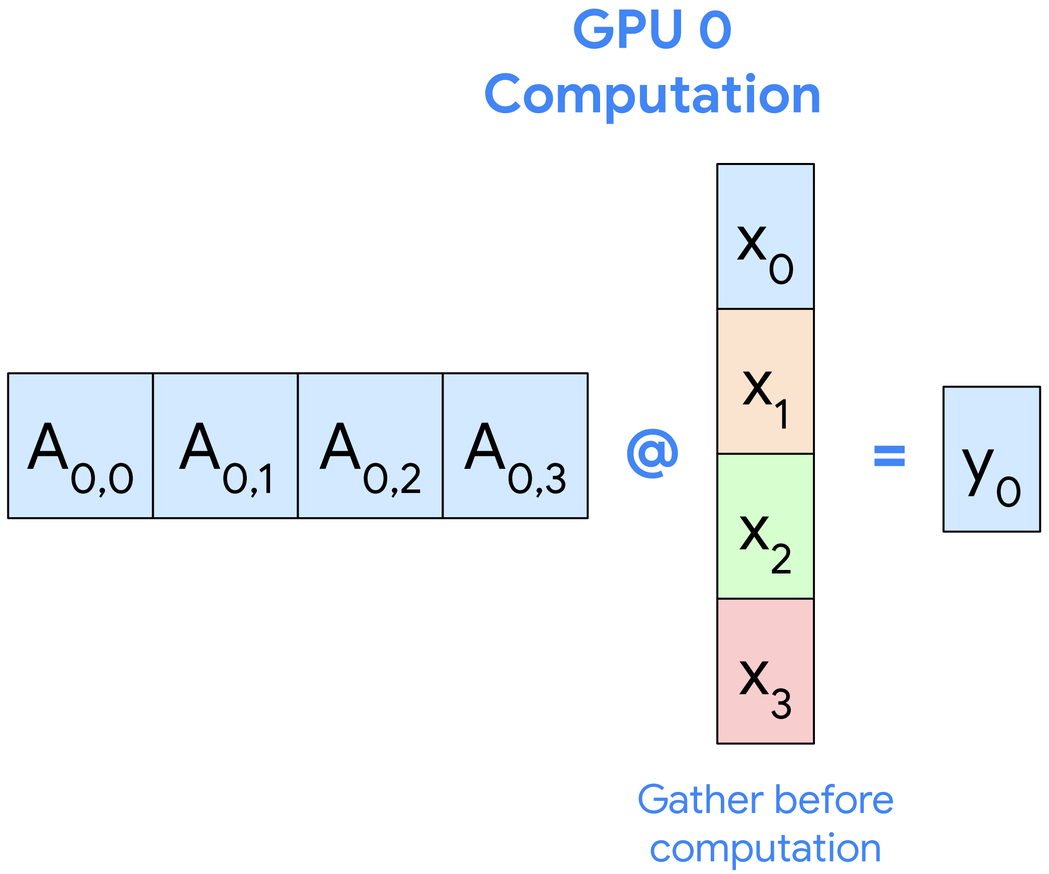
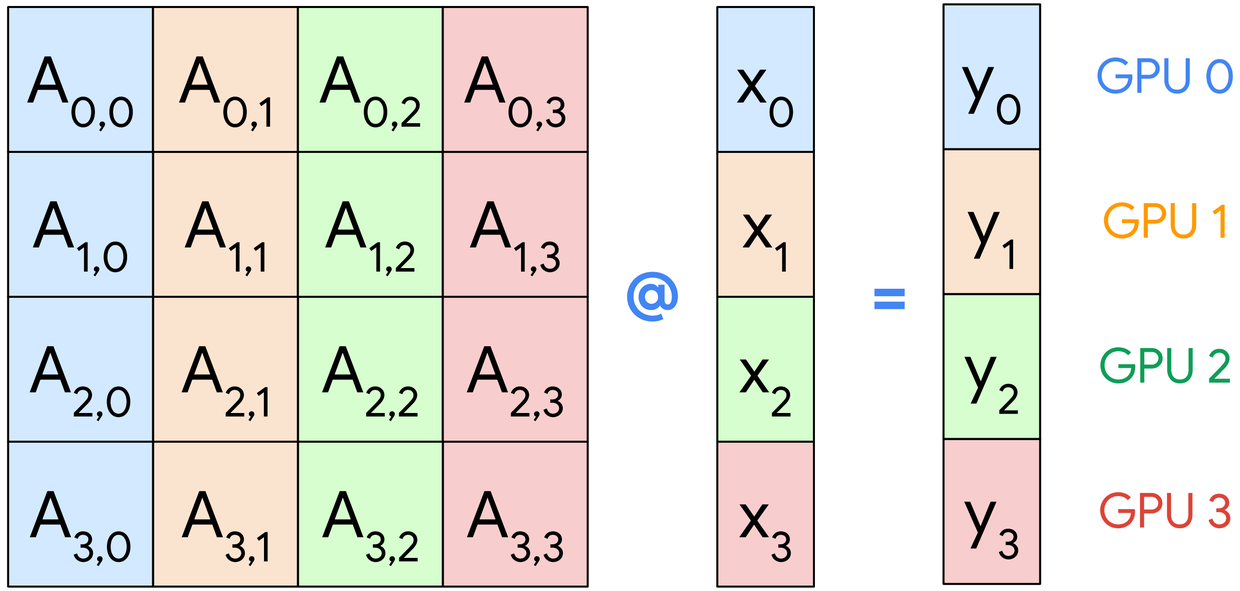


Tensor Parallelism

Linear Layer - Scatter

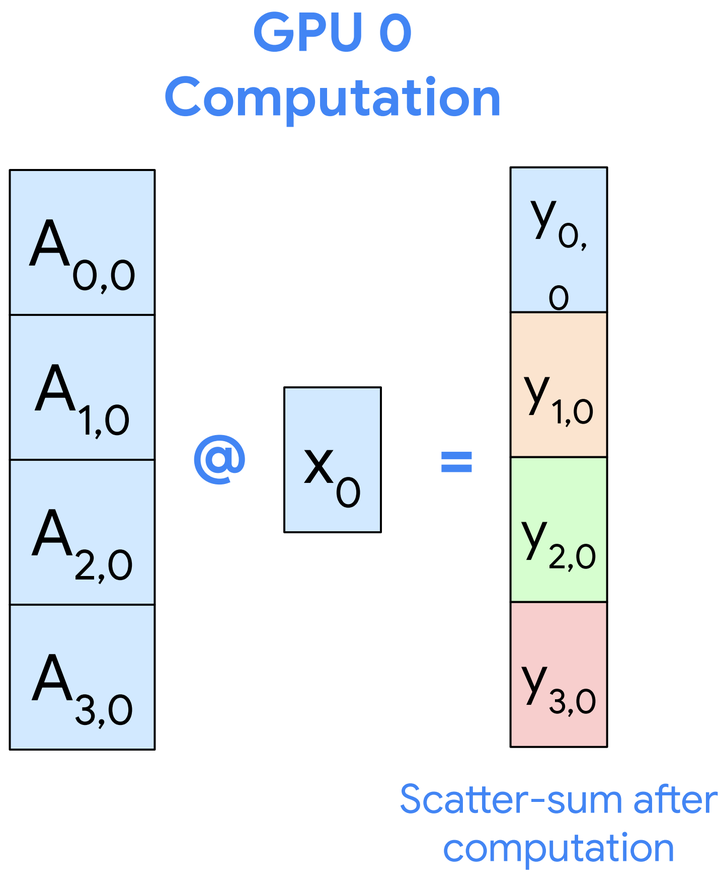
- Matmul of device-own features with device-own parameters give
- Afterwards, **scatter-sum** results to obtain device-own output
- $y_0 = A_{0,0}@x_0 + A_{0,1}@x_1 + A_{0,2}@x_2 + A_{0,3}@x_3$



Tensor Parallelism

Linear Layer - Scatter

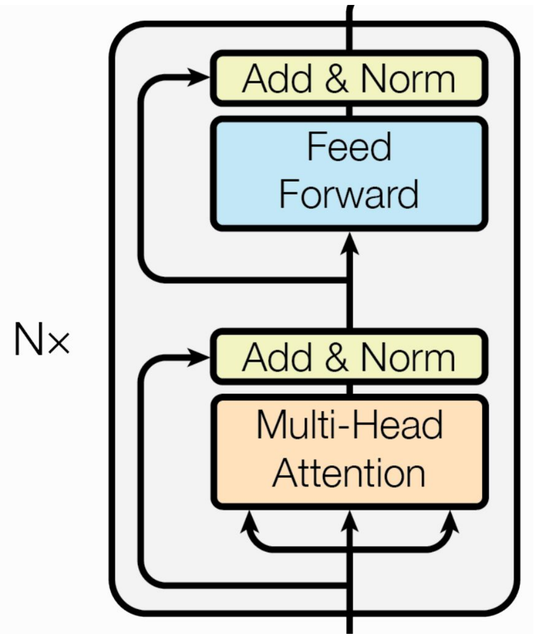
- Matmul of device-own features with device-own parameters give
- Afterward, **scatter-sum** results to obtain device-own output
- $y_0 = y_{0,0} + y_{0,1} + y_{0,2} + y_{0,3}$



Tensor Parallelism

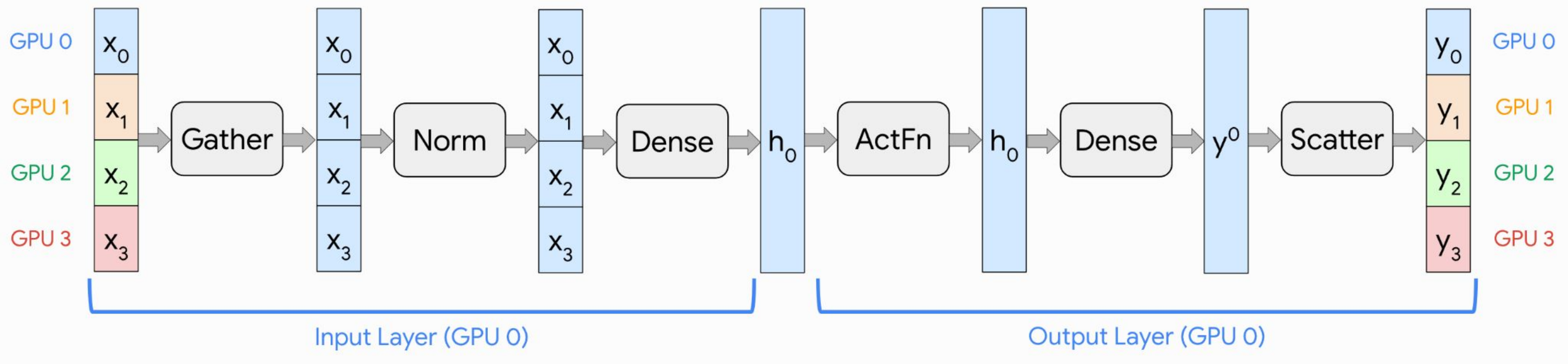
MLP in Transformers

- Select version that communicates the **smallest arrays**
- Example: MLP Block in Transformer
  - Hidden size scales by 4-16x
  - Gather on input layer, scatter on output layer



Tensor Parallelism

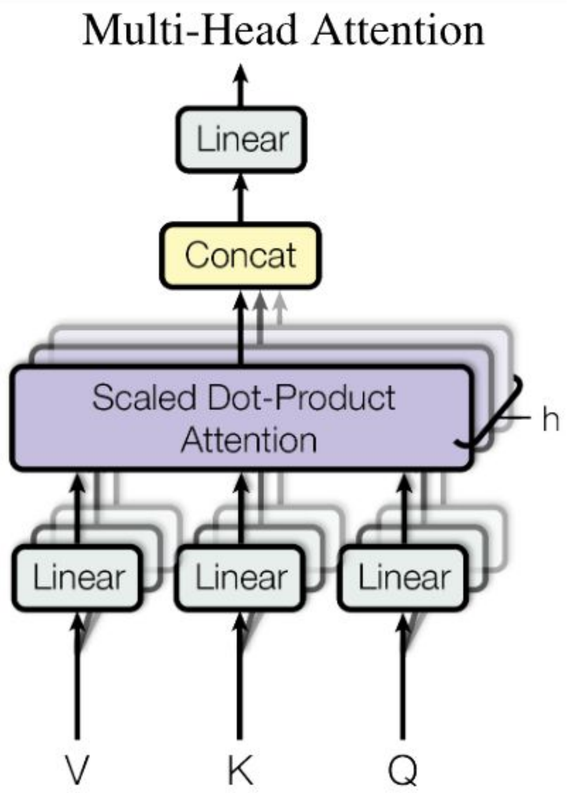
MLP in Transformers



Tensor Parallelism

MHA in Transformers

- Distribute over heads
  a. Gather inputs
  b. Calculate Q, K, V per device-own heads
  c. Calculate self-attention output of device-own heads
  d. Gather/scatter output linear



Tensor Parallelism

Communication Reduction

- Big limitation so far: communication is blocking
  - Devices are idle while waiting for communication
- Reduce by parallelizing Attn and MLP
  - For deep models, similar performance
- Next: Asynchronous Communication

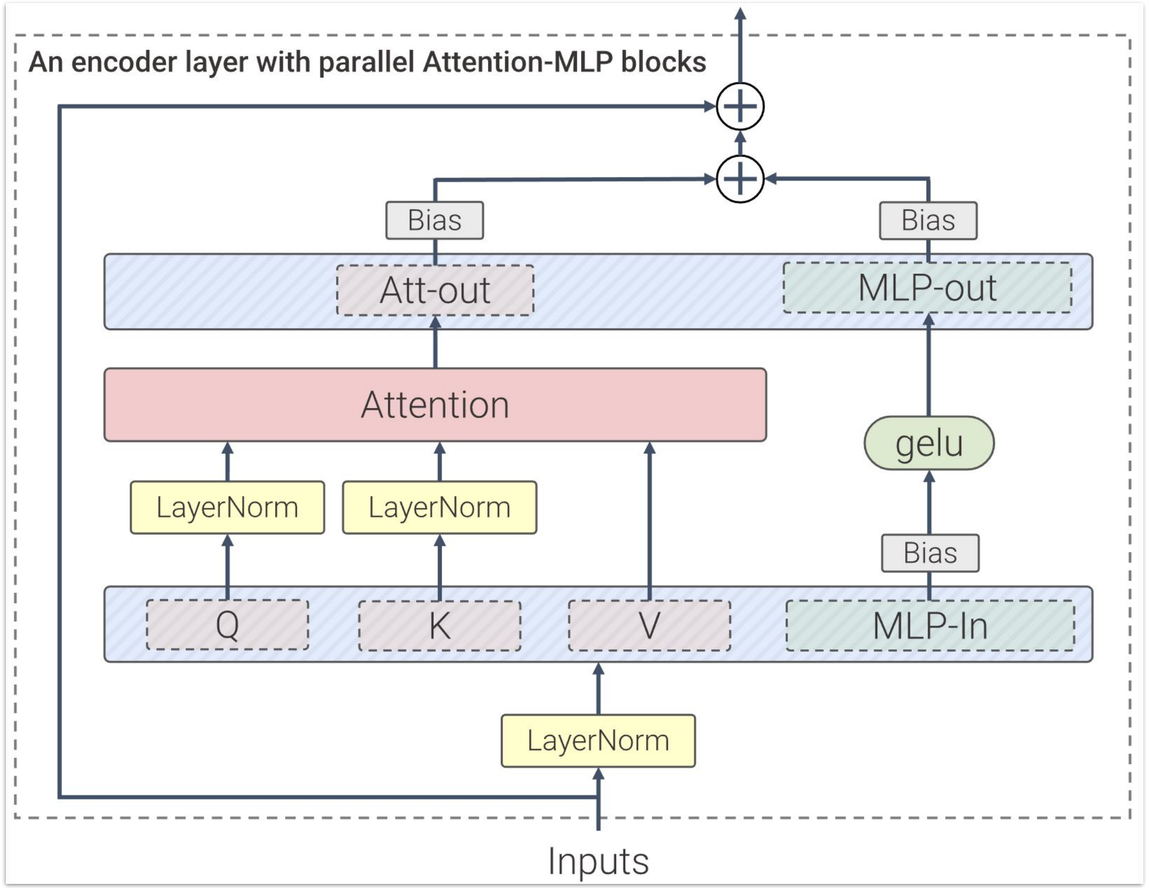


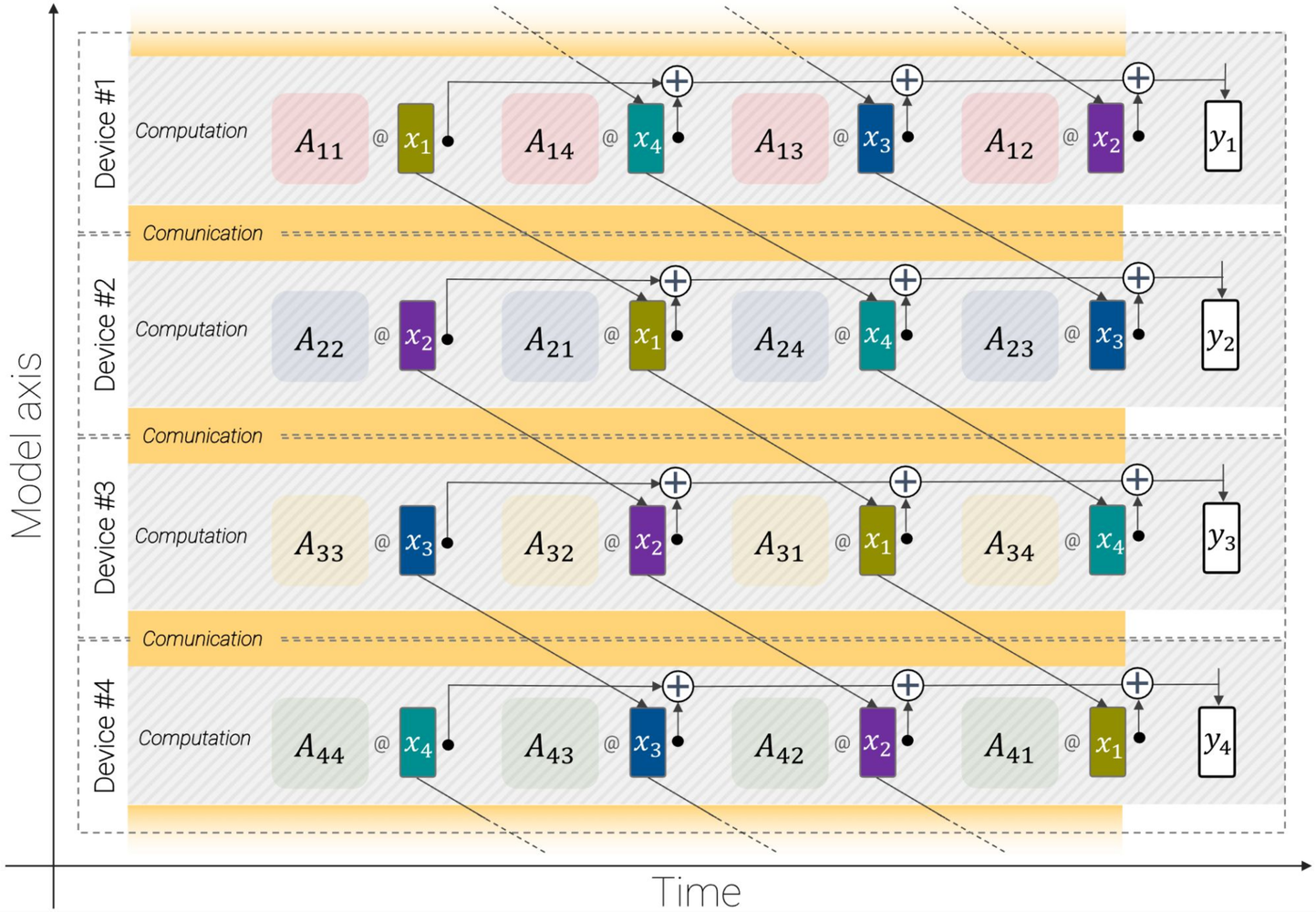
Figure credit: Dehghani et al., 2023

Tensor Parallelism

Asynchronous Layers - Gather

Figure credit: Dehghani et al., 2023

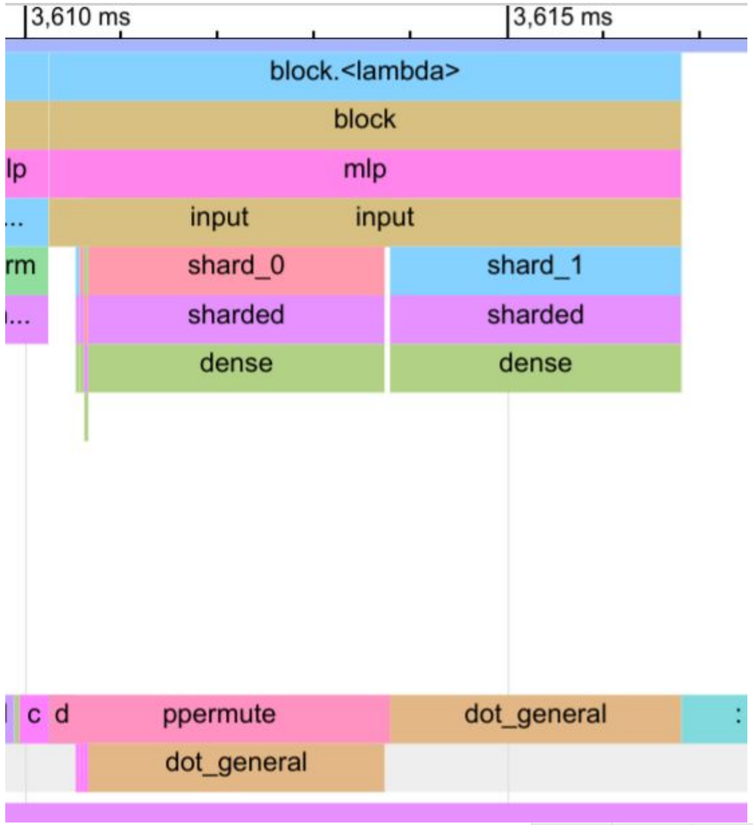
- **Communicate** next feats **while computing** current
- Uses ppermute for fast, ring-based communication
- In ideal case, completely removes communication bottleneck



Tensor Parallelism

Asynchronous Layers - Gather

- Asynchronous communication can be well observed in profile
- 1B LLM trained on 2 A5000 with NVLink 4 (60GB/s)
- Communication blocking negligible

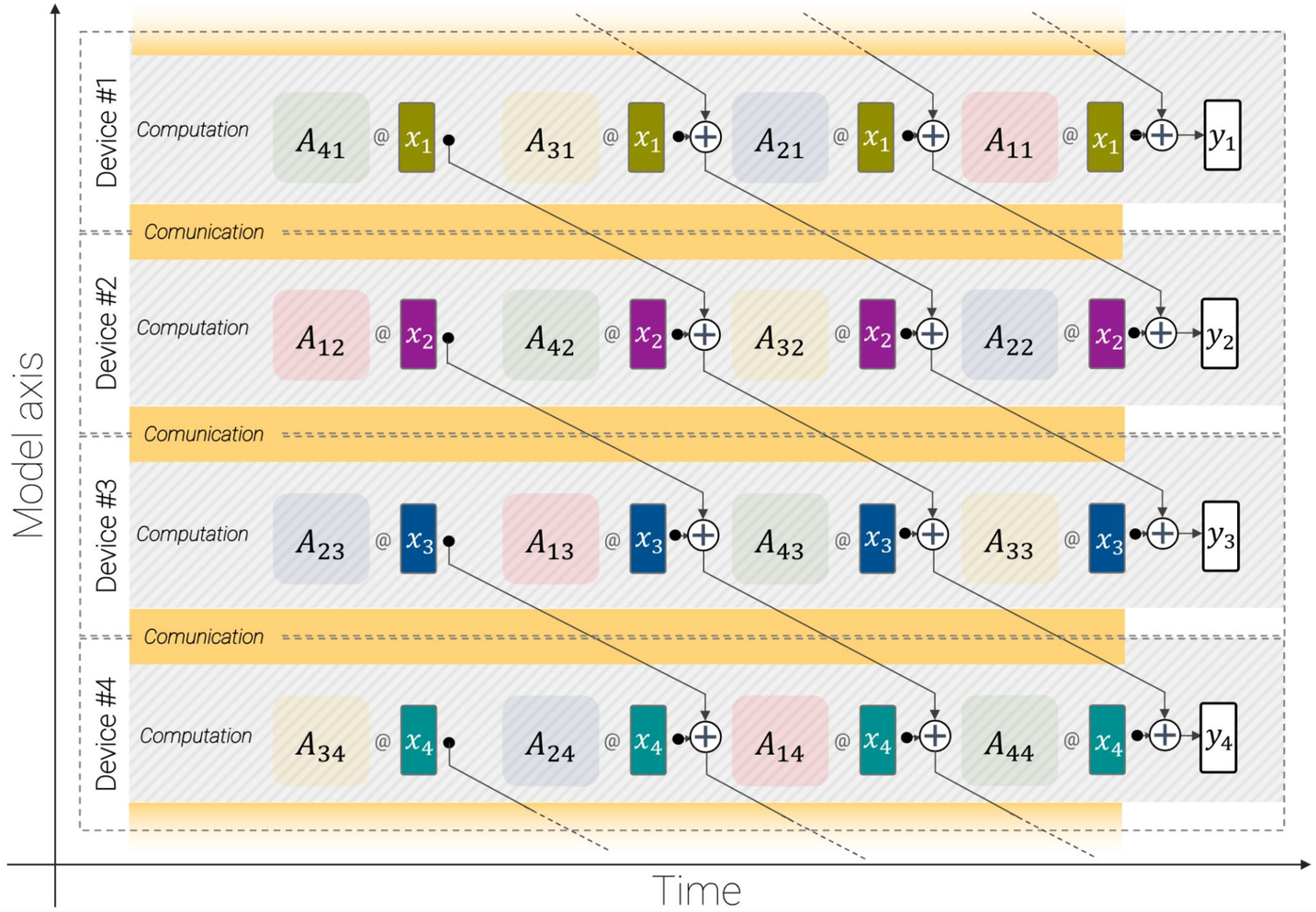


Tensor Parallelism

Asynchronous Layers - Scatter

- First calculate outputs that communicate furthest
- Last compute matmul for device-own output

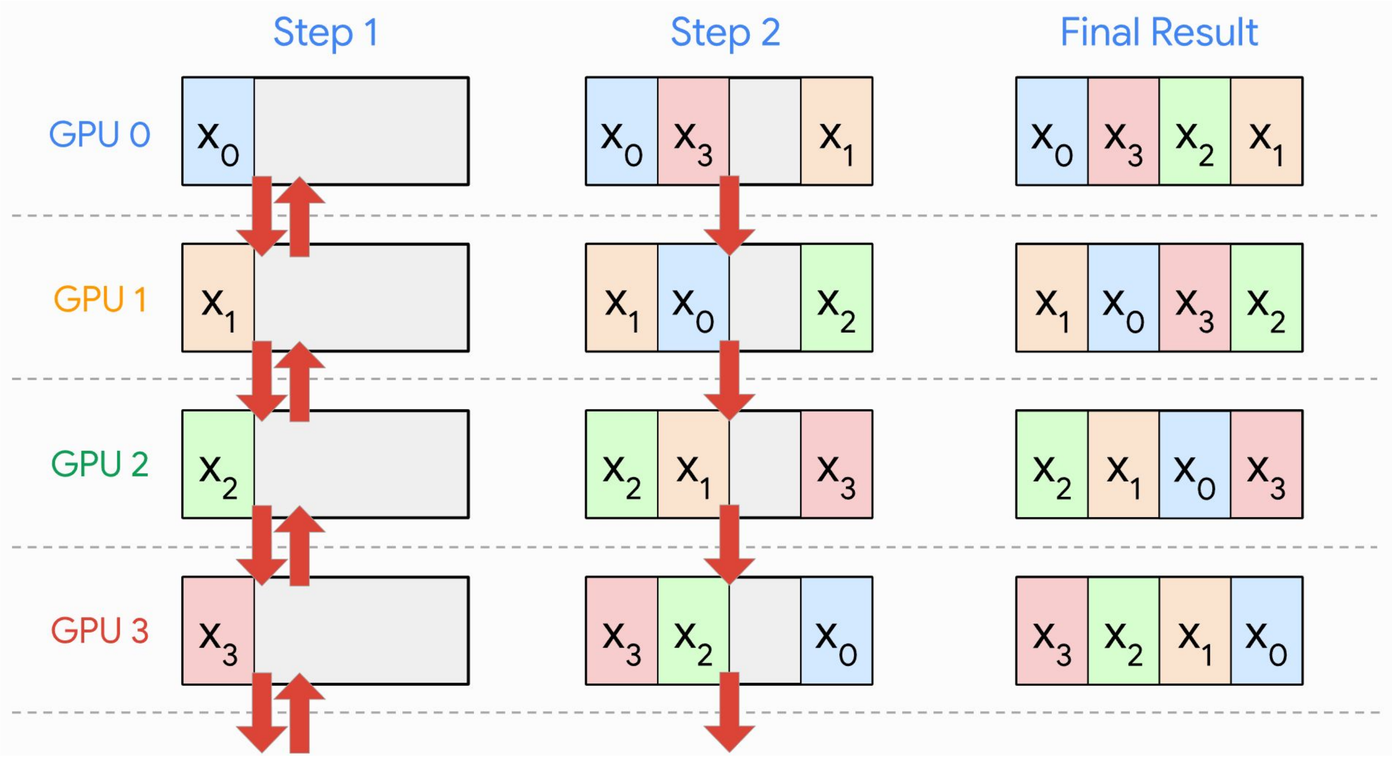
Figure credit: Dehghani et al., 2023



Tensor Parallelism

Asynchronous Layers - Bidirectional

- Device connections are often bidirectional (NVLink, TPUs)
- Can exploit full bandwidth by performing bidirectional communication
- Alternative: split features and comm. half in each direction



Tensor Parallelism

Benefits

- Scales to extremely large models
- Achieves maximum performance with async communication
- Fits well in Single-Program Multiple-Data (SPMD) regime
- Fits well with Transformers

Drawbacks

- Requires high-bandwidth inter-device communications
- Layer-/Model-specific optimization
- More tricky to get model back on single device

3D Parallelism

- Combine all strategies for trillion-parameter scale
- Grouped on bandwidth:
  - Tensor (fastest)
  - Pipeline (intermediate)
  - Data / ZeRO (slow)

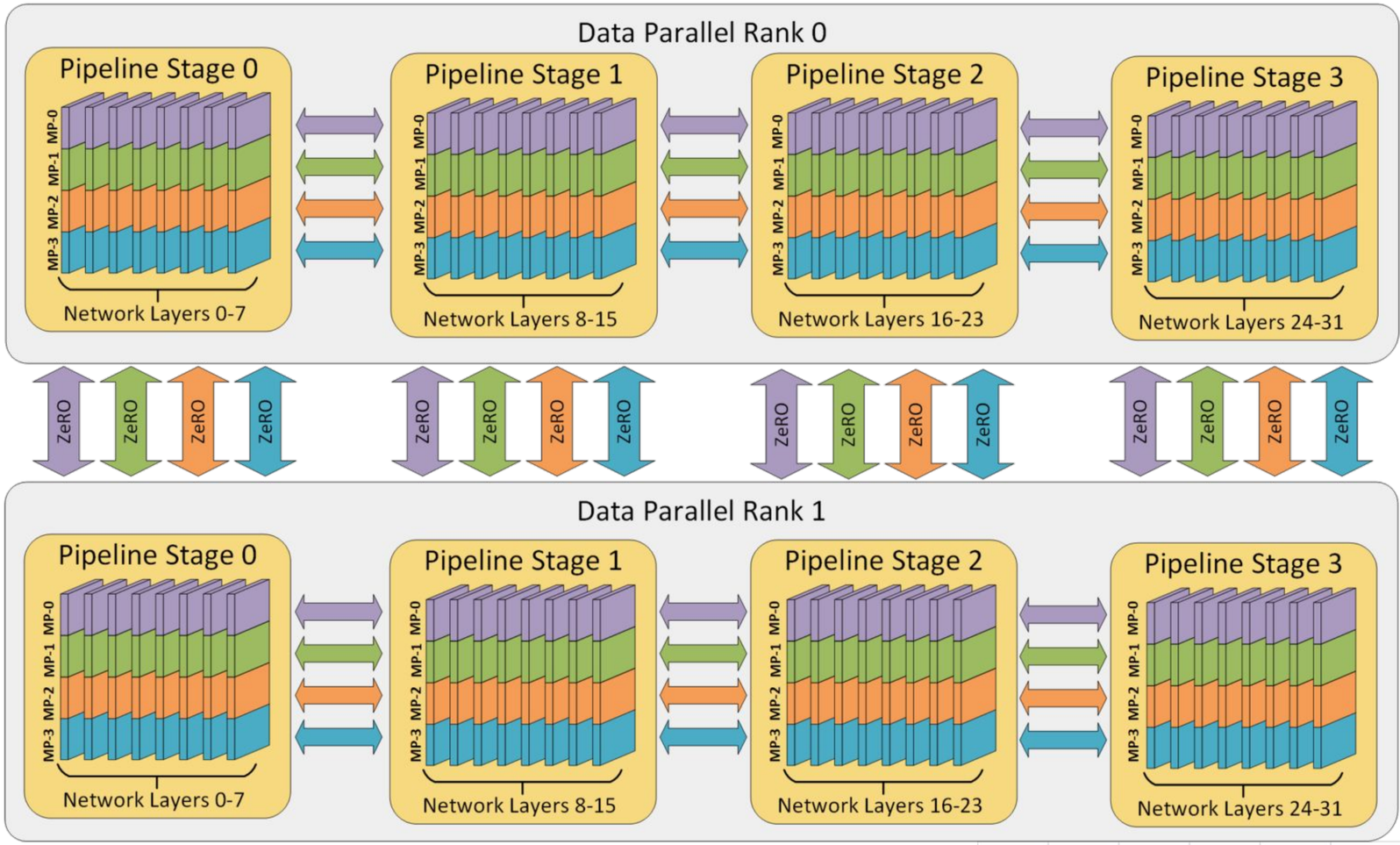


Figure credit: DeepSpeed

3D Parallelism - Nemotron

- Recent NVIDIA Nemotron 340B model trained on 768x8 H100s
  - TP axis size: 8
  - PP axis size: 12
  - DP axis size: 64
    - Batch size 36 per DP element

Figure credit: von Werra

3D Parallelism - Nemotron

- Iteration time multiple seconds
- MFU - Model FLOP/s Utilization

Data-parallel size	GPUs	Iteration time (secs)	MFU (%)	Batch size	Tokens (B)
16	1536	10.3	42.4%	768	200
32	3072	10.3	42.3%	1536	200
64	6144	8.0	41.0%	2304	7600

Figure credit: Nemotron Report

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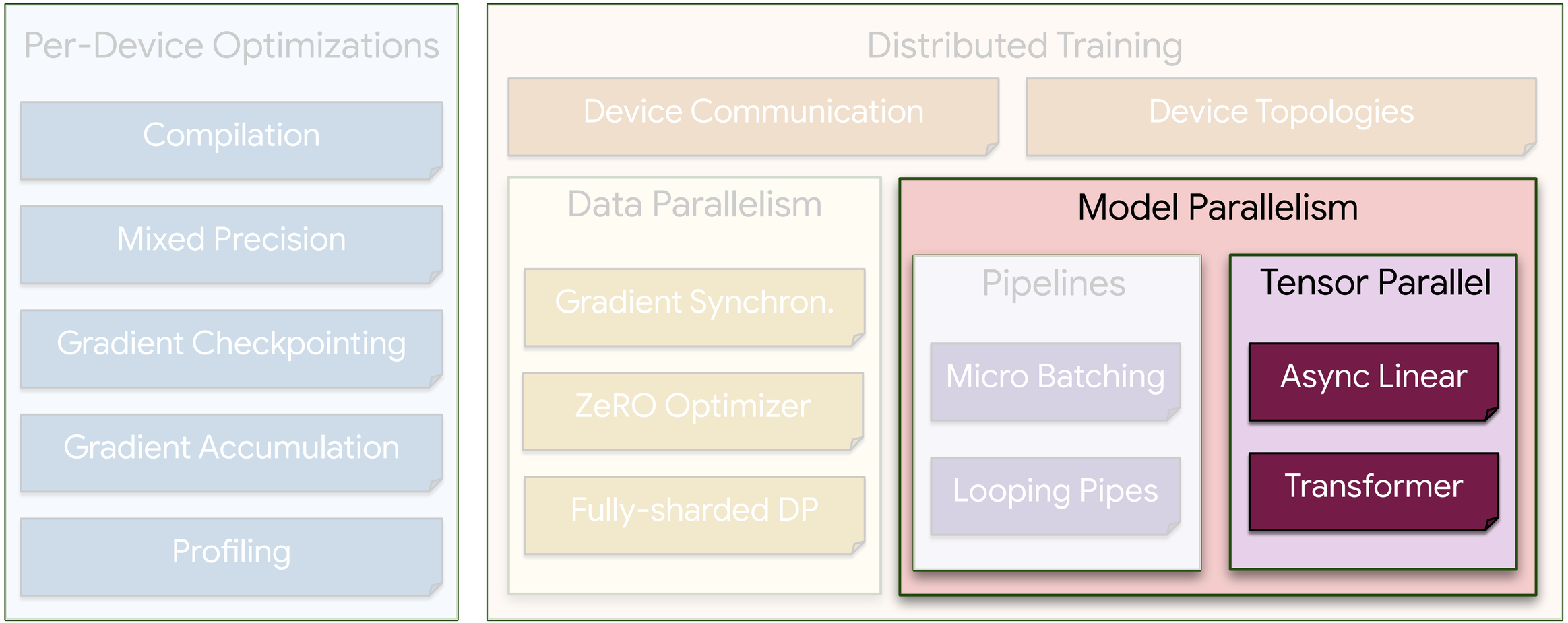
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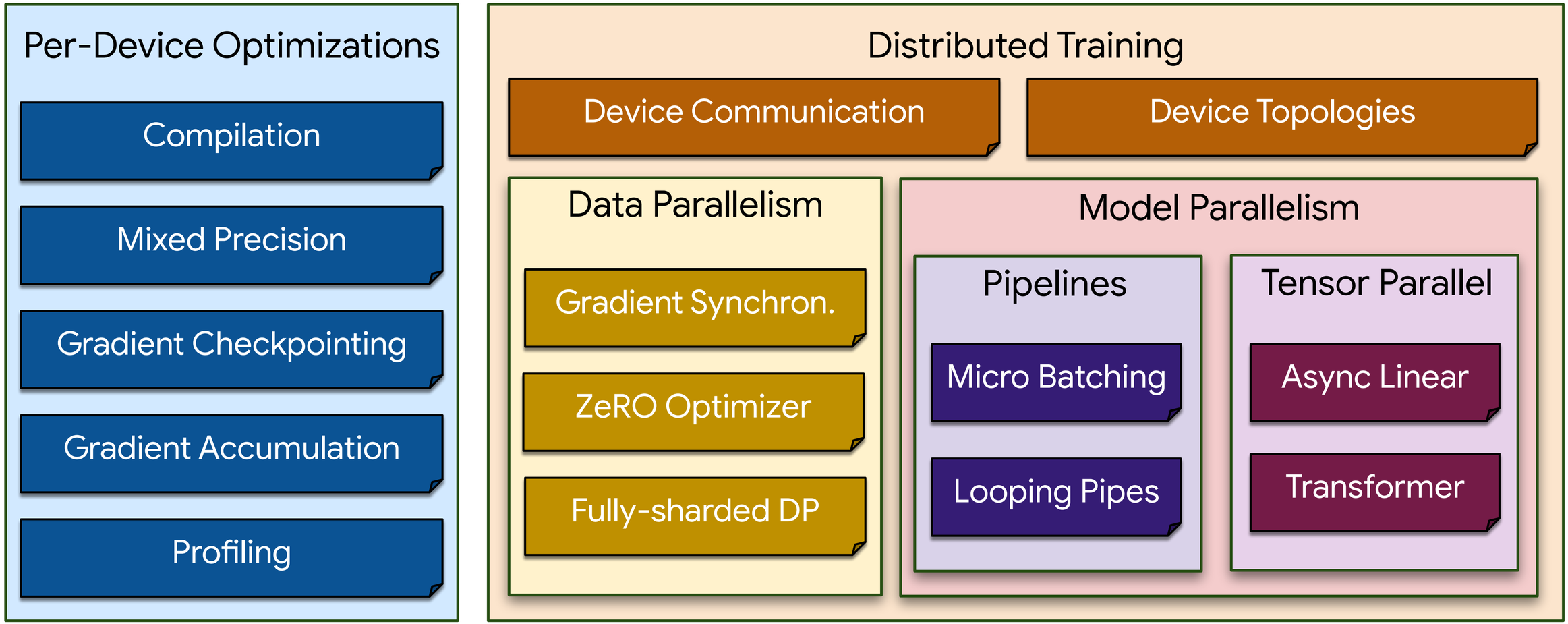
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Summary

Single-Device

- Memory-Compute trade-off on single device
- Mixed precision and compilation to speed-up for “free”
- Profile for bottlenecks

Distributed Training

- Overlapping communication with computation is the key for efficiency
- Small scale: (Fully-Sharded) Data Parallel
- Large scale: Model + Data Parallel
  - Pipeline for intermediate bandwidths
  - Tensor (async) for fast bandwidths
- Tools: DeepSpeed, MaxText
  - Compiler can do a lot of the work

More details:
UvA-DL Notebooks

What we didn’t get to cover

- Sequence parallelism
- Mixture-of-Experts (MoE)
- Implementing own kernel optimizations
- Low-precision optimizers
- Fine-tuning techniques
- Hyperparameter search at scale
- Data loading at scale
- Checkpointing
- Challenges of thousands of GPUs
- And much more...

References and Resources

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Experts

Thank you.

For questions, suggestions, etc.,
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